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Approximate Multipliers Using Static and Dynamic Segmentation: Area, Delay and Power Comparison

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Abstract: *In modern days, the energy efficient and high-speed multipliers are increasing a lot. For the applications where if the arithmetic accuracy is compromised, we use approximate multipliers in order to increase the speed or reduce the power and area, which in effectively means to make the system energy efficient. Approximate multipliers are used in error tolerant applications. Here as an existing work, static segmentation is done for the approximate multipliers and dynamic segmentation is done as modified work. For static segmentation, signed and unsigned multipliers are used. Simple error correction techniques arealso used for signed multipliers. Dynamic controlled input is given for the dynamic segmentation which can be controlled according to the different applications. A comparison is done in the field of area, power, and delay between static and dynamic multipliers. Static and Dynamic approximate multipliers are very promising and effective technique in the field whereerror tolerant applications are allowed. These approximate multipliers are mainly used in image processing applications.*

Key Word: *Static and Dynamic segmentation, Error tolerant, Energy Efficient.*

I.INTRODUCTION

As we know, the request for highly efficient and energy saving systems are readily increasing now a days, The birth of approximate multipliers gave a path to the new era of energy savings, high speed and better area requirements. In the applications such as digital image processing, multimedia processing and data mining, the approximate multipliers are used because they areerror tolerant applications. The block diagram of approximate multiplier is given in the Figure 1.1, there will be a multiplier and multiplicand. According to the requirement of the application,the segmentation will be done. The segmentation can be statically or dynamically according to our application. Then the partial product is generated. After that the partial product reduction or addition will be done. Error correction mechanism is done in order to reduce the maximum error. Then the multiplier product output is obtained.

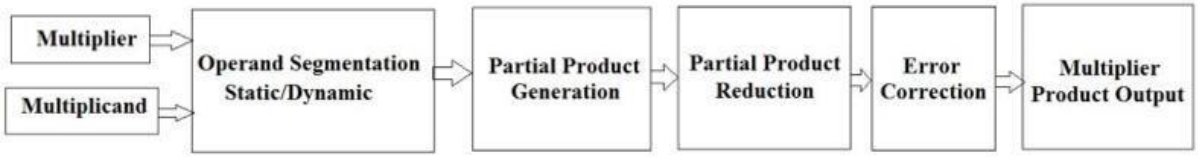

Figure 1.1: Block diagram of approximate multiplier

In these circuits a set of m conterminous bits (a member of m bits) is uprooted from each of thetwo n- bits operand, the two parts are in input to a small m × m internal multiplier whose affairis suitably shifted to gain the result. This is done for both the inked and unsigned multipliers. Suppose we've 8 × 8 multipliers and we will be segmenting into a member of 5 bits. This can be considered as our approximate multiplier and the result can be attained by the partial product reduction. This is substantially used in the operations where the error can be permitted. But if further error occurs, we will be reducing the error by the help of some error reduction system. So, this type of multiplier can be used for the operation where the delicacy isn't important. Thepower, area, detention of the approximate multipliers will be veritably lower than that of the actual multipliers.

II.RELATED WORK AND MOTIVATION

Energy and Quality efficient approximate multipliers with new approximate compressors which provide quality and energy matrices that reduces energy and power dissipation.[1]Comprehensive survey and a comparative evaluation of recently developed approximate arithmetic circuits under different design constraints. Approximation tolerated more in multipliers than in adders and gave high performance and less power dissipation. [2] Multicores and heterogeneous accelerator-based architectures are a by-product of the quest to obtain improvements in the performance of computing platforms at similar or lower power budgets. Itis used in error tolerant applications and the area, power and delay tradeoff takes place. [3] A low-power approximate multiply-accumulate (MAC) unit with reduced area is proposed. [4] Analysis of the architectures of previously proposed compressors to investigate their performance and accuracy. In this article, they propose five high-

accuracy approximate 4-2 compressors [5] A novel inaccurate 4:2 counter that can effectively reduce the partial product stages of the multiplier. [6] A MAC unit, specialized to perform 2D convolution, is designed following the proposed approach and implemented in TSMC 40nm technology in four differentconfigurations. [7] Initial approximate 4:2 compressor that introduces a rather large error to theoutput and the number of faulty rows in the compressor's truth table is significantly reduced byencoding its inputs using generate and propagate signals.[8] The partial products of the multiplier are altered to introduce varying probability terms. Logic complexity of approximation is varied for the accumulation of altered partial products based on their probability.[9] A scalable approximate multiplier, called truncation- and rounding-based scalable approximate multiplier is presented, which reduces the number of partial products by truncating each of the input operands based on their leading one-bit position. [10]

III.EXISTING SYSTEM- STATIC SEGMENTATION

Approximate multipliers are normally used in error tolerant applications. Here the static segmentation method is used in order to do the approximation. Here a detailed analysis of SSM are done and propose some improvements to the basic architecture. The main contributions canbe summarized as follows. Suppose the static segmentation is done for 5 bits, which means the segmentation is set statically to 8 bits. Approximation happens only at LSB bits only then the error is reduced. Segmenting the operand A into LA and HA. HA is 8 bits from MSB and LA is8 bits from LSB. Alpha A is (n-m) MSB bits and Sigma A is (n-m) LSB bits. Checking only thevariation of MSB bits, Alpha A is checked importantly. Because if any variation happens in thesigma A, it will not affect the results badly. Error will be very less. So we can check for alpha

Considering the new approximated multiplier A' which means statically segmenting A intoA' if alpha A is equal to 0, then 4 MSB bits are zeros, A'= LA. If alpha A is not equal to zero, 4MSB bits are non zeros, then A'=HA. This same logic happens in case of operand B also.

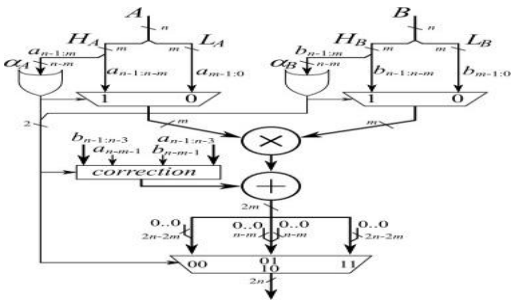

Figure 2.1: Architecture of unsigned Static segmentation with error correction

The above figure shows the architecture of Static segmented multiplier with error correction techniques. A and B are two operands. A is divided into HA and LA. Bis divided into LB and HB. Alpha A is given to OR gate and if alpha A is 0, then the multiplexer will be selecting LA.If alpha A is not zero, then mux will be selecting HA. Same happens with operand B also. Thenit is given to the multiplier unit. Obviously if alpha A is not equal to zero and alpha B is not equal to zero, then HA x HB will be getting and we must go for correction terms, that means d2, d3, d4 is added with the partial products. Suppose we have n=8 and m=5, LA will be from 0 to 4 bit, and HA will be from 3 to 7 bit. Alpha A will be 5^{th}, 6^{th}, and 7^{th}. If all inputs are zero, then alpha A is zero and alpha B is zero. Output will be LA x LB. If alpha A is zero and alphaB is not equal to zero, then output will be LA x HB. If alpha A is not equal to zero, and alpha Bis equal to zero, then output is HA x LB. The correction terms are b n-1 : n-3 and a n-1 : n-3. They are a2 b5, a2 b6, a2 b7, and b2 b5, b2 b6, b2 b7 will be added together. If the mux selecting00, then output will LA x LB. If 01, then output will be LA x HB. If 10, then HA x LB. If 11, then HA x HB.

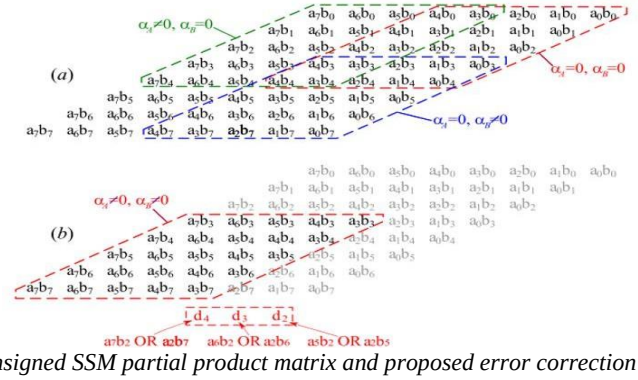

Figure 2.2: Unsigned SSM partial product matrix and proposed error correction (n = 8, m = 5)

IV.PROPOSED SYSTEM-DYNAMIC SEGMENTATION

A hybrid approach is proposed, using a first static segmentation stage and an inner multiplier employing dynamic segmentation. In the existing work, the segmentation was fixed. But in the proposed work, the segmentation is done by dynamically. Inside the fixed part, we areperforming the dynamic segmentation. The segmentation is controlled by dynamic input. Thisdynamic input is dependent on the application.

					X_4 Y_4	X_3 Y_3	X_2 Y_2	X_1 Y_1	X_0 Y_0
					X_4Y_0 D_5	X_3Y_0 D_4	X_2y_0 D_3	X_1Y_0 D_2	X_0y_0 D_1
				X_4Y_1	X_3Y_1 D_5	X_2Y_1 D_4	X_1Y_1 D_3	X_0Y_1 D_2	
			X_4Y_2	X_3Y_2	X_2Y_2 D_5	X_1Y_2 D_4	X_0Y_2 D_3		
		X_4Y_3	X_3Y_3	X_2Y_3	X_1Y_3 D_5	X_0Y_3 D_4			
	X_4Y_4	X_3Y_4	X_2Y_4	X_1Y_4	X_0Y_4 D_5				
P_9	P_8	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0

Suppose X and Y are 5-bit multiplicands. X0, X1, X2, X3, X4 and Y1, Y2, Y3, Y4 are the generated partial products. Dynamic controlled inputs D1, D2, D3, D4, D5 are given to control the products dynamically. From the LSB, D1 is ANDed with X0Y0. D2 is ANDed with X0Y1 and X1Y0. D3 is ANDed with X2Y0, X1Y1 and X0Y2. D4 is ANDed with X3Y0, X2Y1, X1Y2 and X0Y3. D5 is ANDed with X4Y0, X3Y1, X1Y3 and X0Y4

Remaining P5, P6, P7, P8 are MSB bits. So we will not give dynamic input there as they are MSB bits (errors will be more). We can vary the dynamic input using D1 to D5. If we want to truncate last three columns, D1, D2 and D3 can be set to 0. Those three columns will be eliminated. Accordingly depending upon the application, whichever is needed, we can control the dynamic input. Dynamic input with 11111 will be having less error and with 00000 will behaving more error. So based on D value, dynamic segmentation can be performed.

V.POWER, AREA, AND DELAY COMPARISON OVERVIEW

ModelSim software is used for coding and simulating the existing and proposed architectures. ISE Design suites can also be used but the Modelsim software is more user friendly and it has an inbuilt simulation environment which most of the ISE design suites older versions failed to provide. The comparison of area, delay, and power for static and dynamic segmented multipliersis done in Xilinx ISE 8.1i.

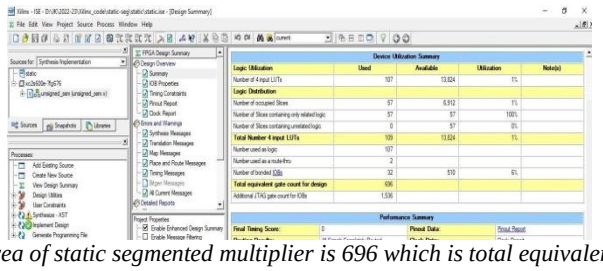

Figure 5.1: Area of static segmented multiplier is 696 which is total equivalent gate count

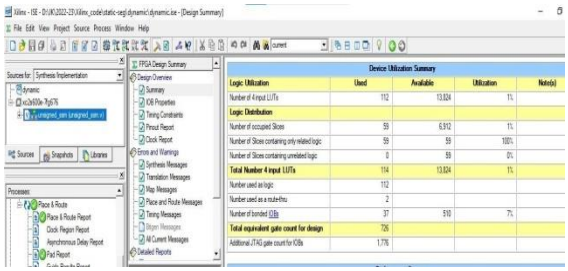

Figure 5.2:Area for Dynamics Segmented Multiplier is 726 Which is total Equivalent Gate Count

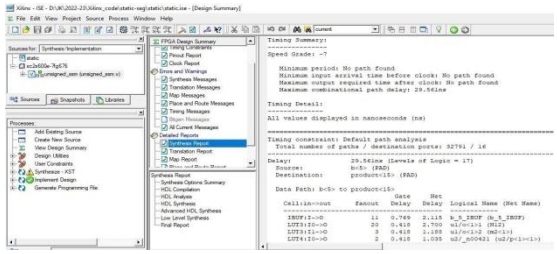

Figure 5.3: Delay for static segmented multiplier is 29.56 ns

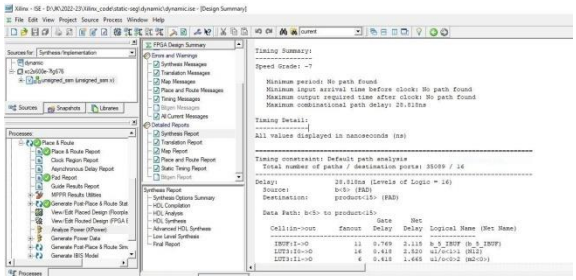

Figure 5.4: Delay of dynamic segmented multiplier is 28 ns

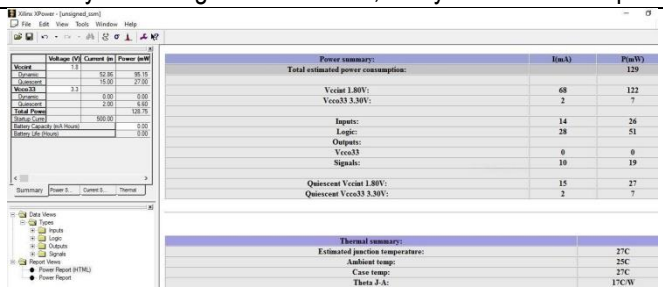

Figure 5.5: Power for static segmented multiplier is 128.76 mW

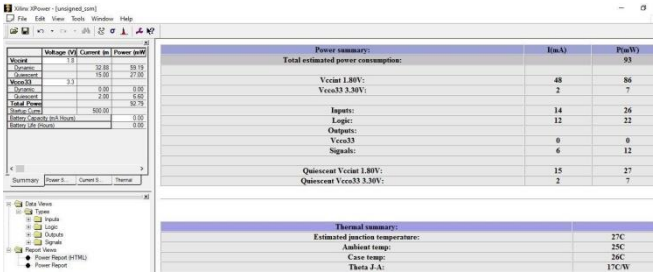

Figure 5.6: Power of dynamic segmented multiplier is 92 mW

VI.CONCLUSION

The approximate multipliers are considered as the emerging technique that achieve these goals. In this project, investigation of approximate multipliers using static segmentation and dynamic segmentation is done. As we know the approximate multipliers are used in error tolerant applications which sacrifices the accuracy of the results for minimizing power or delay or area. In order to reduce the approximation error, simple and effective correction technique is used. These types of multipliers are applicable in many image processing applications where the errorperformance is acceptable. It is done for signed and unsigned multipliers. Modification work is done for dynamic segmentation. This project is done Modelsim and the comparison is done in Xilinx. The comparison in terms of area, delay, and power were done for static and dynamic segmentation. In order to increase the power and reduce the delay or area, and to decrease the hardware complexities, we are mainly used approximate multipliers. For the applications which require less delay and less power, dynamic segmentation multipliers are used. For the applications which require less area, static multipliers are used. Depending upon the applicationwe can decide how to use the circuits whether it is taken for static segmentation or dynamic segmentation by the comparison of area, delay, and power.

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