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Novel Design of Ternary Arithmetic Circuits

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Abstract: *Over the few decades, complementary metal oxide semiconductor technology has led to thedevelopment of digital systems. However, the dimension scaling of CMOS approach is limit, to overcome this disadvantage carbon nano tube FETS (CNTFETs) are came into existence. Here changing of the thresholdvoltageofthe CNTFETs are possible by varyingitsdimensions(length, width). They enable new paradigms in circuit designs, such as muti valued logic(MVL). These circuits focus on minimizing the hardware cost by processing more than twovalues per elementary operation. Therefore, it reduces the inter connection complexity ofdigitalsystemscomparedthat ofbinary logiccircuits.*

Arithmetic circuits are playing an important key role in many electronic systems suchasmicroprocessorsanddigitalsignalprocessorswithhighefficiency.Theefficiencyofthesystemsare mainlyevaluatedbytheirarithmeticcircuit'scapability.WiththehelpoftheseCNTFETS, the design of arithmetic circuits like half adder and multiplier will be proposedTheaboveproposedhalfadderand multiplieris simulatedby usingtheH-spicesoftware.

Keywords *- Multi-valued logic,ternary logic circiuts,CNTFET's,Nanotubes*

I. INTRODUCTION

Very large-scale Integration (VLSI) is the process of creating an integrated circuit (IC) by combining millions of MOS transistors onto a single chip. VLSI began in the 1970s when MOSintegrated circuit chips were widely adopted, enabling complex semiconductor and telecommunication technologies to be developed. The microprocessor and memory chips are VLSI devices. Before the introduction of VLSI technology, most ICs had a limited set of functions they could perform. An electronic circuit might consist of a CPU, ROM, RAM and glue logic. VLSI lets IC designers add all of these into one chip.

General Microelectronics introduced the first commercial MOS integrated circuit in 1964. In the early 1970s, MOS integrated circuit technology allowed the integration of more than 10,000transistors in a single chip. This paved the way for VLSI in the 1970s and 1980s, with tens ofthousands of MOS transistors on a single chip (later hundreds of thousands, then millions, andnow billions).

The first semiconductor chips held two transistors each. Subsequent advances added more transistors, and as a consequence, more individual functions or systems were integrated over time. The first integrated circuits held only a few devices, perhaps as many as ten diodes, transistors, resistors and capacitors, making it possible to fabricate one or more logic gates ona single device. Now known retrospectively as small-scale integration (SSI), improvements intechnique led to devices with hundreds of logic gates, known as medium-scale integration (MSI). Further improvements led to large-scale integration (LSI), i.e. systems with at least a thousand logic gates. Current technology has moved far past this mark and today's microprocessors have many millions of gates and billions of individual transistors.

At one time, there was an effort to name and calibrate various levels of large-scale integrationabove VLSI. Terms like ultra-large scale integration (ULSI) were used. But the huge number of gates and transistors available on common devices has rendered such fine distinction moot.Terms suggesting greater than VLSI levels of integration are no longer in widespread use.

In 2008, billion-transistor processors became commercially available. This became more commonplace as semiconductor fabrication advanced from the then-current generation of 65nm processors. Current designs, unlike the earliest devices, use extensive design automationand automated logic synthesis to lay out the transistors, enabling higher levels of complexity in the resulting logic functionality. Certain high- performance logic blocks like the SRAM (static random-access memory) cell, are still designed by hand to ensure the highest efficiency.

1.1 History Of Scale Integration:

The electronics industry has achieved a phenomenal growth over the last two decades, mainlydue to the rapid advances in

integration technologies, large-scale systems design - in short, dueto the advent of VLSI. The number of applications of integrated circuits in high performance computing, telecommunications, and consumer electronics has been rising steadily, and at a very fast pace. Typically, the required computational power (or, in other words, the intelligence) of these applications is the driving force for the fast development of this field. Figure 1.3 gives an overview of the prominent trends in information technologies over the nextfew decades. The current leading-edge technologies (such as low bit-rate video and cellular communications) already provide the end-users a certain amount of processing power and portability. This trend is expected to continue, with very important implications on VLSI and systems design. One of the most important characteristics of information services is their increasing need for very high processing power and bandwidth (in order to handle real-time video, for example). The other important characteristic is that the information services tend tobecome more and more personalized (as opposed to collective services such as broadcasting),which means that the devices must be more intelligent to answer individual demands, and at the same time they must be portable to allow more flexibility/mobility.

The level of integration as measured by the number of logic gates in a monolithic chip has beensteadily rising for almost three decades, mainly due to the rapid progress in processing technology and interconnects technology. Table 1.1 shows the evolution of logic complexity in integrated circuits over the last three decades, and marks the milestones of each era. Here, the numbers for circuit complexity should be interpreted only as representative examples to show the order-of-magnitude. A logic block can contain anywhere from 10 to 100 transistors,depending on the function. State-of-the-art examples of ULSI chips, such as the DEC Alpha or the INTEL Pentium contain 3 to 6 million transistors.

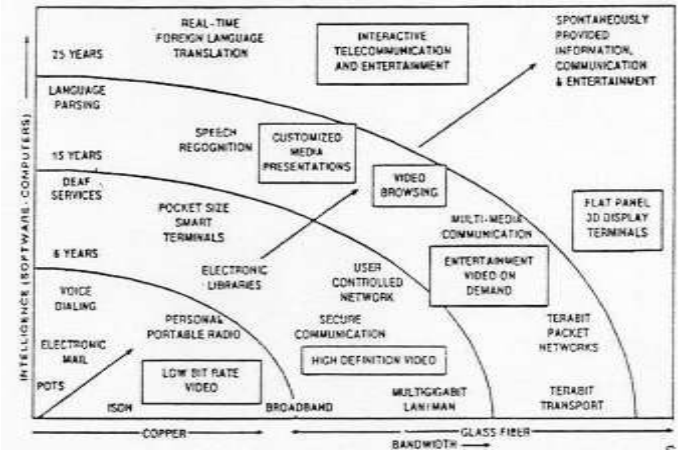


Figure1: prominent trends in information service technologies.

1.2 Carbon Nano Tubes:

Diamond and graphite are considered as two natural crystalline forms of pure carbon. In diamond, carbon atoms exhibit hybridization, in which four bonds are directed towards the corners of a regular tetrahedron. The resulting three-dimensional network (diamond) is extremely rigid, which is one reason for its hardness. In graphite, hybridization occurs, in which each atom is connected evenly to three carbons (120°) in the plane, and a weak bond ispresent in the axis. The set forms the hexagonal (honeycomb) lattice typical of a sheet of graphite. A new form of carbon, Buckminster fullerene (C_{60}), was discovered in 1985 by a team headed by Korto and coworkers. Besides diamond, graphite, and fullerene (C_{60}), quasione-dimensional nanotube is another form of carbon first reported by Ijima in 1991 whenhe discovered multiwalled carbon nanotubes (MWCNTs) in carbon soot made by an arc discharge method. Carbon nanotubes (CNTs) are allotropes of carbon. CNTs are tubular inshape, made of graphite. The tubes contained at least two layers, often many more, and rangedin outer diameter from about 3 nm to 30 nm. About two years later, he made the observation of single-walled carbon nanotubes (SWCNTs). At about the same time, Dresselhaus et al. synthesized single-walled carbon nanotubes by the same route of producing MWCNTs but adding some transition metal particles to the carbon electrodes. The single walled nanotubes are generally narrower than the multi-walled tubes, with diameters typically in the range 1- 2 nm, and tend to be curved rather than straight. A significant amount of work has been done in the past decade to reveal the unique structural, electrical, mechanical, electromechanical, and chemical properties of CNTs. Recent research has focused on improving the quality of catalytically-produced nanotubes.

While nanotubes of other compositions exist, most research has been focused on the carbon ones. Therefore, the “carbon” qualifier is often left implicit in the acronyms, and the names areabbreviated NT, SWNT, and MWNT.

The length of a carbon nanotube produced by common production methods is often not reported, but is typically much larger than its diameter. Thus, for many purposes, end effects are neglected and the length of carbon nanotubes is assumed infinite.

Carbon nanotubes can exhibit remarkable electrical conductivity, while others are semiconductors. They also have exceptional tensile strength and thermal conductivity because of their nanostructure and strength of the bonds between carbon atoms. In addition, they can be chemically modified. These properties are expected to be valuable in many areas of technology, such as electronics, optics, composite materials (replacing or complementing carbon fibers), nanotechnology, and other applications of materials science.

Rolling up a hexagonal lattice along different directions to form different infinitely long single-wall carbon nanotubes shows that all of these tubes not only have helical but also translationalsymmetry along the tube axis and many also have nontrivial rotational symmetry about this axis.

A special group of a chiral single-wall carbon nanotubes are metallic, but all the rest are eithersmall or moderate band gap semiconductors. These electrical properties, however, do not depend on whether the hexagonal lattice is rolled from its back to front or from its front to backand hence are the same for the tube and its mirror image.

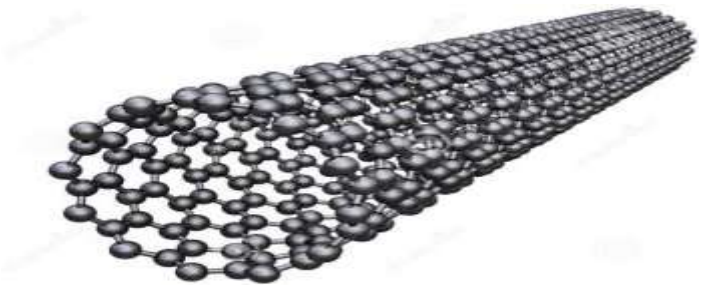


Figure 2: Carbon Nanotube

1.3 Types Of Cnts:

Carbon nanotubes are classified in following two types: SWCNTs—Single-walled carbon nanotubes and MWCNTs—Multiple-walled carbon nanotubes. Comparison between SWCNTand MWCNT is as presented in Table 1.2.

Table 1:Comparison between SWCNT and MWCNT

SWCNT	MWCNT
Single layer of graphene.	Multiple layer of graphene
Catalyst is required for synthesis.	Can be produced without catalyst.
Bulk synthesis is difficult as it requires propercontrol over growth and atmospheric condition.	Bulk synthesis is easy.
Not fully dispersed , and form bundled structures.	Homogeneously dispersed with no apparentbundled formation.
Resistivity usually in the range of 10^{-4}-$10^{-3}\Omega$m.	Resistivity usually in the range of $1.8*10^{-5}$ to$6.1*10^{-5}$ Ω-m.
It can be easily twisted and more pliable.	It cannot be easily twisted.
A chance of defect is moreduring functionalization.	A chance of defect is less especially whensynthesized by discharged method.
Characterization and evaluation is easy	It has very complex nature.

Comprised entirely of carbon, the structure of pure SWCNT can be visualized as rolled-up tubular shell of graphene sheet which is made up of benzene type hexagonal rings of carbon atoms (Figure 3). Graphene sheets are seamless cylinders derived from a honeycomb lattice,representing a single atomic layer of crystalline graphite. A MWCNT is a stack of graphene sheets rolled up into concentric cylinders. Each nanotube is a single molecule composed of millions of atoms and the length of this molecule can be tens of micrometers long with diameters as small as 0.7 nm. The SWCNTs usually contain only 10 atoms around the circumference and the thickness of the tube is only one-atom thick.

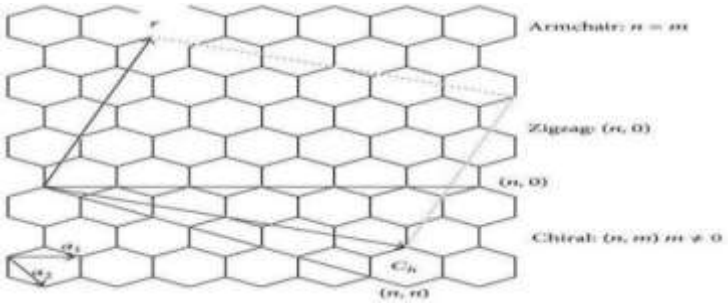


Figure 3: Schematic representation of formation of single-walled carbon nanotubes byrolling of a grapheme sheet along lattice vectors which leads to armchair, zigzag, andchiral tubes

II .CARBON NANOTUBES

A carbon nanotube field-effect transistor (CNTFET) is a field-effect transistor that utilizes a single carbon nanotube or an array of carbon nanotubes as the channel material instead of bulksilicon in the traditional MOSFET structure. First demonstrated in 1998, there have been majordevelopments in CNTFETs since.

A carbon nanotube's bandgap is directly affected by its chiral angle and diameter. If those properties can be controlled, CNTs would be a promising candidate for future nano-scale transistor devices. Moreover, because of the lack of boundaries in the perfect and hollow cylinder structure of CNTs, there is no boundary scattering. CNTs are also quasi-1D materialsin which only forward scattering and back scattering are allowed, and elastic scattering meansthat free paths in carbon nanotubes are long, typically on the order of micrometers. As a result,quasi-ballistic transport can be observed in nanotubes at relatively long lengths and low fields.Because of the strong covalent carbon–carbon bonding in the sp^2 configuration, carbonnanotubes are chemically inert and are able to transport large electric currents. In theory, carbonnanotubes are also able to conduct heat nearly as well as diamond or sapphire, and because oftheir miniaturized dimensions, the CNTFET should switch reliably using much less power thana silicon-based device.

2.1 Device Fabrication:

There are many types of CNTFET devices; a general survey of the most common geometries are covered below.

2.1.1 Back-gated CNTFETs:

The earliest techniques for fabricating carbon nanotube (CNT) field-effect transistors involvedpre-patterning parallel strips of metal across a silicon dioxide substrate, and then depositing theCNTs on top in a random pattern. The semiconducting CNTs that happened to fall across two metal strips meet all the requirements necessary for a rudimentary field-effect transistor. One metal strip is the "source" contact while the other is the "drain" contact. The silicon oxide substrate can be used as the gate oxide and adding a metal contact on the back makes the semiconducting CNT gateable.

This technique suffered from several drawbacks, which made for non-optimized transistors. The first was the metal contact, which actually had very little contact to the CNT, since the nanotube just lay on top of it and the contact area was therefore very small. Also, due to the semiconducting nature of the CNT, a Schottky barrier forms at the metal–semiconductor interface, increasing the contact resistance. The second drawback was due to the back-gate device geometry. Its thickness made it difficult to switch the devices on and off using low voltages, and the fabrication process led to poor contact between the gate dielectric and CNT.

Top View **Side View**

Figure 4: Top and side view of a silicon back-gated CNTFET

2.1.2 Top-gated CNTFETs:

Eventually, researchers migrated from the back-gate approach to a more advanced top-gate fabrication process. In the first step,

single-walled carbon nanotubes are solution deposited ontoa silicon oxide substrate. Individual nanotubes are then located via atomic force microscope orscanning electron microscope. After an individual tube is isolated, source and drain contacts are defined and patterned using high resolution electron beam lithography. A high temperatureanneal step reduces the contact resistance by improving adhesion between the contacts and CNT. A thin top-gate dielectric is then deposited on top of the nanotube, either via evaporationor atomic layer deposition. Finally, the top gate contact is deposited on the gate dielectric, completing the process.

Arrays of top-gated CNTFETs can be fabricated on the same wafer, since the gate contacts areelectrically isolated from each other, unlike in the back-gated case. Also, due to the thinness ofthe gate dielectric, a larger electric field can be generated with respect to the nanotube using a lower gate voltage. These advantages mean top-gated devices are generally preferred over back-gated CNTFETs, despite their more complex fabrication process.

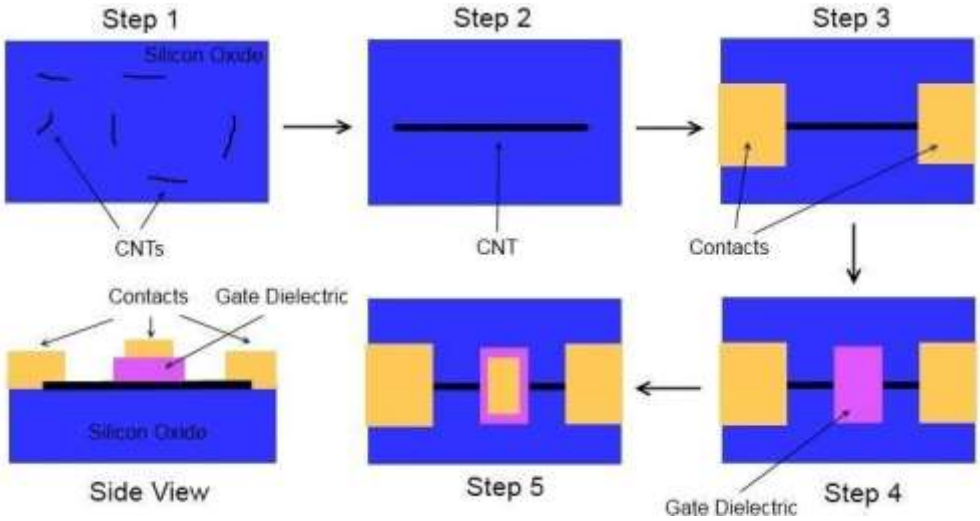


Figure 5: The process for fabricating a top-gated CNTFET

2.1.3 Wrap-around gate CNTFETs:

Wrap-around gate CNTFETs, also known as gate-all-around CNTFETs were developed in 2008, and are a further improvement upon the top-gate device geometry. In this device, insteadof gating just the part of the CNT that is closer to the metal gate contact, the entire circumference of the nanotube is gated. This should ideally improve the electrical performanceof the CNTFET, reducing leakage current and improving the device on/off ratio.

Device fabrication begins by first wrapping CNTs in a gate dielectric and gate contact via atomic layer deposition. These wrapped nanotubes are then solution-deposited on an insulatingsubstrate, where the wrappings are partially etched off, exposing the ends of the nanotube. Thesource, drain, and gate contacts are then deposited onto the CNT ends and the metallic outer gate wrapping.

:

Figure 6: Sheathed CNT

2.1.4 Suspended CNTFETs:

Yet another CNTFET device geometry involves suspending the nanotube over a trench to reduce contact with the substrate and gate oxide. This technique has the advantage of reducedscattering at the CNT-substrate interface, improving device performance. There are many methods used to fabricate suspended CNTFETs, ranging from growing them over trenches using catalyst particles, transferring them onto a substrate and then under-etching the dielectricbeneath, and transfer-printing onto a trenched substrate.The main problem suffered by suspended CNTFETs is that they have very limited material options for use as a gate dielectric (generally air or vacuum), and applying a gate bias has the effect of pulling the nanotube closer to the gate, which places an upper limit on how much thenanotube can be gated. This technique will also only work for shorter nanotubes, as longer tubes will flex in the middle and droop towards the gate, possibly touching the metal contact and shorting the device. In general, suspended CNTFETs are not practical for commercial applications, but they can be useful for studying the intrinsic properties of clean

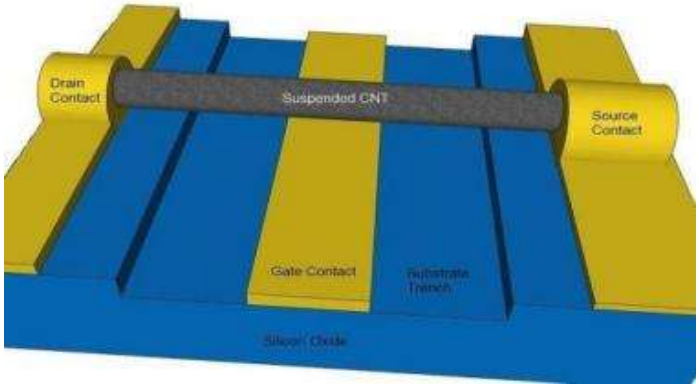


Figure 7: A suspended CNTFET device

III.TERNARY LOGIC

3.1 Introduction To Ternary Logic:

The fundament of today's digital technology age is binary logic. The time when Shannon expressed the behaviour of electrical switches on Boolean algebra, he overlay the ramp to an industrial development which is recognized as beginning of one of the most revolutionary economic changes ever.

Binary logic technology has come across the dramatic changes and advances. Earlier from electro-mechanical to electronic switches by using electronic tubes like triode, pentodes, thenfrom tubes to transistors and from transistors to LSI and VLSI circuits. Although efficient andpowerful, binary logic is not the most efficient and powerful switching logic. Non-binary logicor Many Valued Logic or Many Valued Logic.

The subject of MVL is also known as Multi-Valued, Multiple-Valued or Many-Valued Logic.In case of 3-Valued logic the term 'Ternary' logic is used and term 'Quaternary' logic for 4Valued logic and so on up to 'n' values. Multi-Value logic is regarded as a switch with morethan two states. Such as a 3-value switch logic states '0','1' and '2', 4-value switch with logicstates '0','1','2' and '3' and so on up to 'n values.

In existing binary digital system, the output of the system is decided by considering two inputconditions i.e. either ON (Favourable or true logical level 1) or OFF (Unfavourable or false logic at logic level 0) leaving behind the third conditions i.e. when both the input conditions are same. As specified in the SQL standard, ternary logic, or three-valued logic, is a logic system with three truth values: TRUE, FALSE, AND UNKNOWN. Ternary logic applies to the evaluation of Boolean expressions, as well as predicates, and effects the results of logical operations such as AND, OR, and NOT.

MVL (Multi-Valued Logic) is also called as Multiple Valued, Multi-Valued logic. MVL that is, Multi-Valued Logic is termed as a technique that has more than two possible states or two truth values. A two-valued logic can be extended to a n-valued logic, that is, for example, in athree valued logic i.e., base or radix as three, it is termed as ternary logic and a quaternary logic i.e., radix as four is used for four valued Logic and so on. Such a three value logic with logic symbols as 0,1 and 2 and four valued logic has logic states of 0,1,2 and 3.

The ternary numeral system has its base or radix as 3. Radix generally defined as the number of unique digits or unique symbols that can be expressed using a single digit. In a binary system, the two logic symbols 0 and 1 are used to represent a value, and coming to the ternarysystem, the three logic symbols (0, 1 and 2) are used. The bipolar notation is one of the methodsin the ternary logic system which is denoted with symbols -1, 0, 1. In this paper, the notation used is 0,1 and 2. The ternary logic system gives the meaning of three-valued switching. Threevalued logic system or ternary logic system has many benefits when compared with the binarylogic system in designing digital circuits. reduction in chip area can be achieved, and more importantly, easy error detection and error correction codes can be employed.

For instance, more data can be transmitted over an arrangement of lines in a given length, diminishing in the complexity of interconnections is observed, decrease in chip area can be accomplished, and more significantly the error detection and error correction of codes can be accomplished.

The ternary logic system has some significant merits over the binary logic system [2,3]. To implement the different logic functions, the decrease in the number of interconnections in a circuit is observed, in this way, the chip area has been reduced, and importantly more data canbe transmitted and lesser memory is required. Apart from this, at very higher speeds, the serialand some serial-parallel operations are carried out. It's been used in applications like areas of communications and digital signal processing.

As ternary logic we will mean a system L whose elements called propositions or statements are valued in the set {0, 1, 2}. This set we denote by Z3. If x is a proposition, the value of x can be seen as a mapping ν : L → {0, 1, 2} such that; ν(x) = 1; if x is true 0; if x is perhaps true, perhaps false 2; if x is false From this, we have that if ν(x) = 1 (true) under the rules of binary logic then also ν(x) = 1(true) under the ternary logic laws. Analogously for the false value. On the other hand, for the same considerations made for binary logic case, we can avoidν by making ν(x) = x.

3.2 Types Of Cntfet Based On Ternary Logic:

In ternary logic circuits, transistors with different threshold voltages are required for implementation of basic ternary gates like NTI, PTI, encoder, decoder etc. Unlike in MOS technology, where body biasing is used to control threshold voltages, in CNFET technology the threshold voltage is controlled by changing the diameter (i.e. Vth dependent on physical dimension) of CNT which in turn depends on the chirality vector. This dependence makes CNTFET suitable for implementation of MVL circuits. While interest in design of CNFET based logic circuits waned over recent years due to complex fabrication technology and reliability issues. STI (simple ternary inverter), PTI (positive ternary inverter) and NTI (Negative ternary inverter) are the three basic ternary elements.

3.2.1 Standard Ternary Inverter:

The working of STI is, if the input voltage Vin is 0volts (logic 0), then NMOS becomes off and PMOS becomes on, as a result, there will be no flow of current in resistors and the outputbecomes logic 2(i.e., 1.8 volts). On contrary, if the input voltage is 1.8 volts (logic 2), then NMOS becomes turned on and PMOS is turned off, which impacts as, there will be no flow ofcurrent in the resistors and the output becomes logic 0(i.e., 0 volts). And if the input voltage is0.9volts (logic 1), which is equal to VDD/2 voltage level, both PMOS and NMOS become turned on and consequently current could flow in both the resistors. The resistors R value is 1mega ohm are chosen such that it should be much.

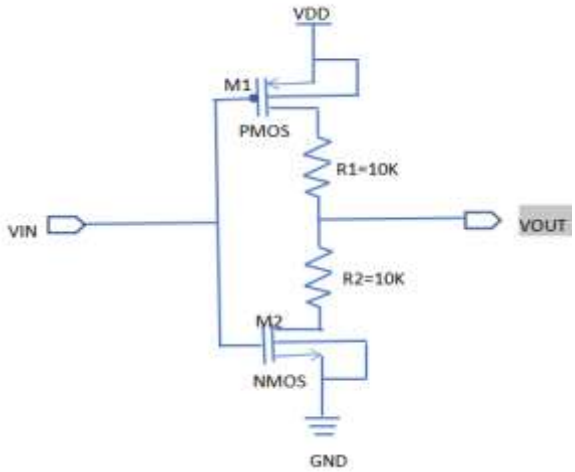


Figure 8: Schematic circuit diagram of simple ternary inverter

The present invention relates to a ternary logic circuit, and more particularly, to a ternary logiccircuit which uses a junction BTBT leakage current and a threshold current mechanism in an off state to create a ternary logic gate in the same circuit configuration as a CMOS- to a ternarylogic circuit capable of increasing the density. Conventional binary logic based digital systems have focused on increasing the bit density of information through the miniaturization of CMOS devices in order to process large amounts of data quickly. However, recently, integration into 30-nm or less has been limited byincreasing the bit density due to the increase of leakage current and power consumption due toEspecially, as a basic unit for implementing a ternary logic, STI) has been actively developed.However, unlike conventional binary inverters which use two CMOSs as one voltage source, the prior arts related to STI have a problem in that they require more voltage sources or requirea complicated circuit configuration.

3.2.2.Positive Ternary Inverter:

The schematic of a positive ternary inverter is shown in below Figure In the case of PTI, wheninput Vin reaches to 0 volts (logic 0) then the output is 1.8 volts (logic2) because at this time PMOS is turned on, since this path acts like a close path and the total voltage drop appears at the output terminal is 1.8 volts. When input Vin=0.9 volts or (logic 1) then output equals 1.8 volts or appeared as a logic 2. When input appears as 1.8 volts or as a logic 2 the PMOS gate to source terminal is open. As a result, the output appears as 0 volts.

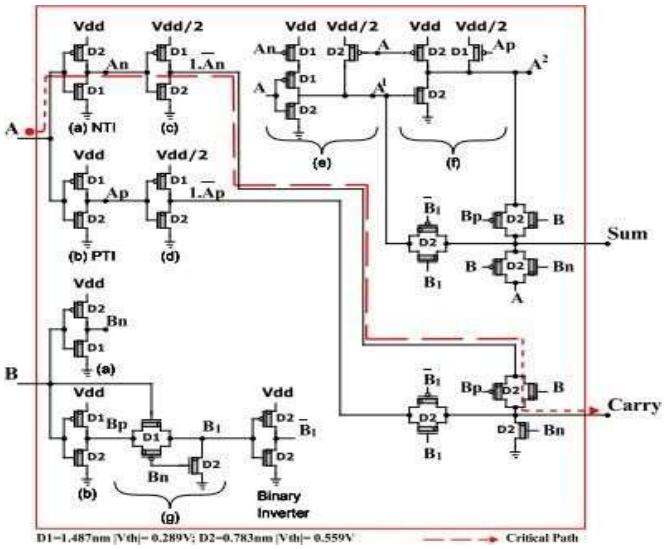


Figure 9:Schematic circuit diagram Positive ternary inverter

3.2.3 Negative Ternary Inverter:

The circuit diagram of the negative ternary inverter is shown in Figure 2.3. When Vin =0.9v or1.8v, NMOS is ON. Current will always conduct when there will be a channel i.e., Vgs > Vt (threshold voltage), gives the voltage of the circuit. So, output as low as 0 volts (logic 0) up to1.8v.

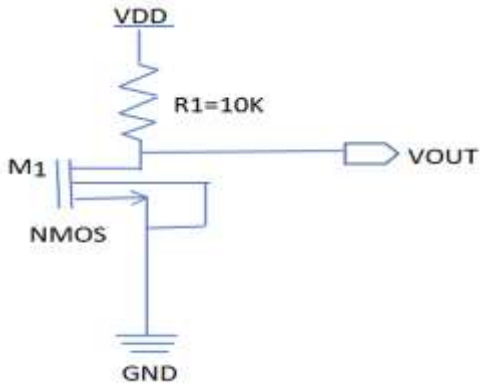


Figure10 Schematic diagram of negative ternary inverter

IV.IMPLEMENTATION OF TERNARY LOGIC CIRCUITS

Two major problems are facing the embedded systems and nano-scale circuits currently, which are the CMOS (Complementary Metal Oxide Semiconductor) transistor, and the binary circuits. Solutions can be done by using CNTFET (Carbon Nano-Tube Field Effect Transistor) instead of CMOS transistor andusing MVL (Multiple-Valued Logic) circuits instead of binary circuits.

(1) The CMOS faces significant complications in nanotechnology circuits such as tight channel-effects and high current leakage. Therefore, many scientists proposed various alternative solutions in the transistor technologies like FinFET (Fin Field-Effect Transistor), Spin-wave, Single electron devices, CNTFET. Among all different transistor technologies, CNTFET has a higher performance.

(2) The binary circuits require high energy consumption. Whereas, MVL circuits reduce the consumption ofenergy because the MVL digit can hold over two states of data. The ternary system (Low: 0 (0V), Middle:1 (Vdd/2), and High: 2 (Vdd)), which is designed and implemented in this work, has a higher performancesystem among all known base systems.

Many researchers implement MVL in several applications like Machine learning and IoT, Algorithm, Data transmission, Healthcare, Combined with binary circuits, Resistive RAM or Memristor, Ternary Converters, and ternary circuits. However, the challenge in the ternary circuit is-How to obtain the logicalstate 1 (Vdd/2) from one power supply (Vdd)? Many researchers inserted two resistors (which increase the size of the circuit and are not recommendedin VLSI circuits) and others inserted two diode-connected transistors acting like resistors to solve the problem size in VLSI.

Use ternary unary operators that can replace the basic logic gates, which significantly reduce the numberof used transistors and energy consumption. So, the transistors count can be reduced, decrease the energy consumption, improve the robustness toprocess variations, and noise tolerance.

4.1 TERNARY HALF ADDER: 1-trit THA can add two ternary inputs (A,B) and produces two outputs: the Sum and the Carry, as described in truth Table.

Figure 10: Ternary Half adder

The proposed THA with 35 CNTFETs: (a) NTI, (b) PTI, (c) 1 · A¯n, (d) 1 · A¯ p, (e) A 1, (f) A 2, and (g) the proposed B . Using Unary operators-based design. When the voltage supply (Vdd) decreases in a transistor then the propagation delay willincrease. Therefore, any pathfrom inputs to outputs contains transistors that have voltage supply equalto Vdd/2, that path will have higher propagation than other paths that have voltage supply equal Vdd.

Table 1: The truth table of THA

Sum

A/B	B_0 (0)	B_1 (1)	B_2 (2)
A_0 (0)	0	1	2
A_1 (1)	1 } **A**	2 } $\mathbf{A^1}$	0 } $\mathbf{A^2}$
A_2 (2)	2	0	1

Carry

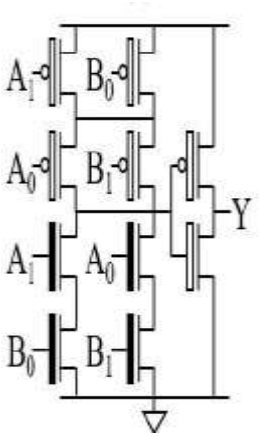
A/B	B_0 (0)	B_1 (1)	B_2 (2)
A_0 (0)	0	0	0
A_1 (1)	0 } **0**	0 } $1 \cdot \overline{A_p}$	1 } $1 \cdot \overline{A_n}$
A_2 (2)	0	1	1

where Ai and Bi , i ∈ {0,1,2}.

$$\begin{aligned} Sum &= 2 \cdot (A_0B_2 + A_1B_1 + A_2B_0) \\ &\quad +1 \cdot (A_0B_1 + A_1B_0 + A_2B_2) \\ Carry &= 1 \cdot (A_1B_2 + A_2B_1 + A_2B_2) \qquad (2) \\ Sum &= A.B_0 + (1.A_0 + 2.A_1 + 0.A_2).B_1 \\ &\quad +(2.A_0 + 0.A_1 + 1.A_2).B_2 \\ Carry &= 0.B_0 + (0.A_0 + 0.A_1 + 1.A_2).B_1 \\ &\quad +(0.A_0 + 1.A_1 + 1.A_2).B_2 \qquad (3) \\ Sum &= A.B_0 + A^1.B_1 + A^2.B_2 \\ Carry &= 0.B_0 + (1 \cdot \bar{A_p}).B_1 + (1 \cdot \bar{A_n}).B_2 \qquad (4) \end{aligned}$$

The above equations shows the proposed THA with 35 CNTFETs using eight unaryoperators, transmission gates (TGs), and dual-voltages (Vdd, Vdd/2). Without using cascading TGs, which is the advantage compared to THA with 34 CNTFETs in thatused cascading TGs. Because cascading TGs provide higher propagation delays andenergy consumption.

4.2 Ternary Multiplier: 1-trit multiplier can multiply two ternary inputs(A, B) and produces two outputs: the product and the Carry, as described in truth Table.



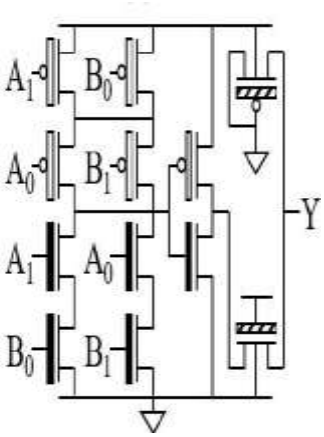


Figure11:Product gate Figure 12: Carry gate

Figures shows the proposed TMUL with CNTFETs using four unary operators ,dual-voltages(Vdd, Vdd/2)the input A to the output Product via (A, Ap, ¯A2 , TG (B, Bp), then Product), when A changes from 1 to 2, B = 2, and Product from 2 to 1.

Table 2: The truth table of multiplier

Product

A/B	B_0 (0)	B_1 (1)	B_2 (2)	
A_0 (0)	0	0	0	
A_1 (1)	0	1	2	$\overline{A^2}$
A_2 (2)	0	2	1	

A

Carry

A/B	B_0 (0)	B_1 (1)	B_2 (2)
A_0 (0)	0	0	0
A_1 (1)	0	0	0
A_2 (2)	0	0	1

$$Product = 2\cdot(A_1B_2 + A_2B_1) + 1\cdot(A_1B_1 + A_2B_2)$$

$$Carry = 1\cdot A_2B_2 \quad (5)$$

$$Product = 0.B_0 + A.B_1 + (0.A_0 + 2.A_1 + 1.A_2).B_2$$

$$Carry = 0.B_0 + 0.B_1 + (0.A_0 + 0.A_1 + 1.A_2).B_2 \quad (6)$$

$$Product = 0\cdot B_0 + A\cdot B_1 A + \bar{A^2}B_2$$

$$Carry = 0\cdot B_0 + 0\cdot B_1 + (1\cdot \bar{A_p})B_2 \quad (7)$$

The equations of the product and the Carry can be obtained fromTable2 to lead threedifferent designs:

V.SIMULATION AND RESULTS

5.1 SIMULATION OF TERNARY HALF ADDER:

Below are the output waveforms of the ternary half adder. These waveforms are obtained by using theH-spice software

Figure13:Waveforms for the input value ‘A’ v(a)

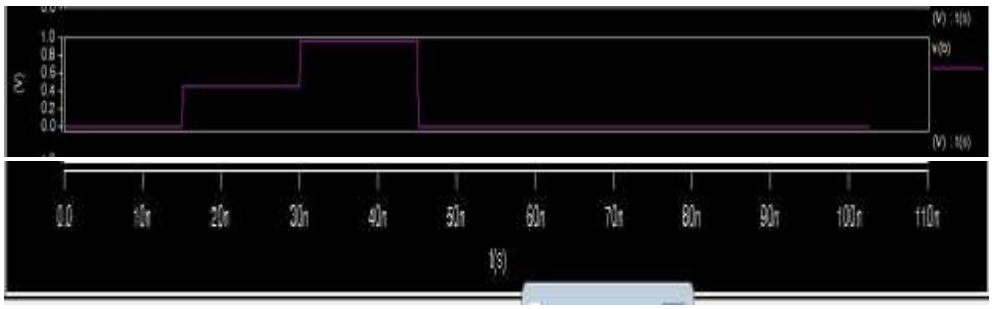


Figure14: Waveform for the input value ‘B’ v**(b)**

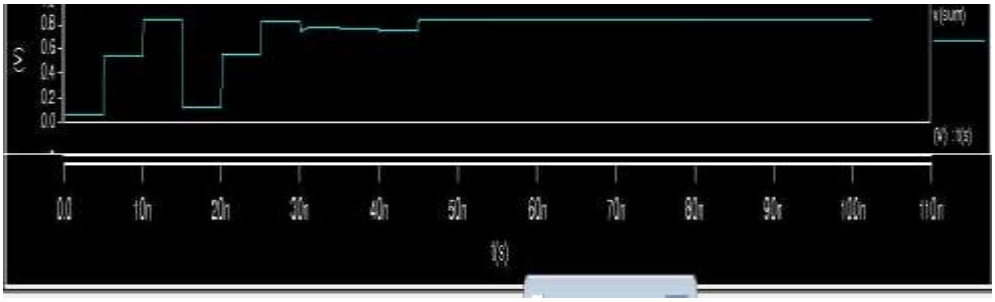


Figure15: Sum output waveform

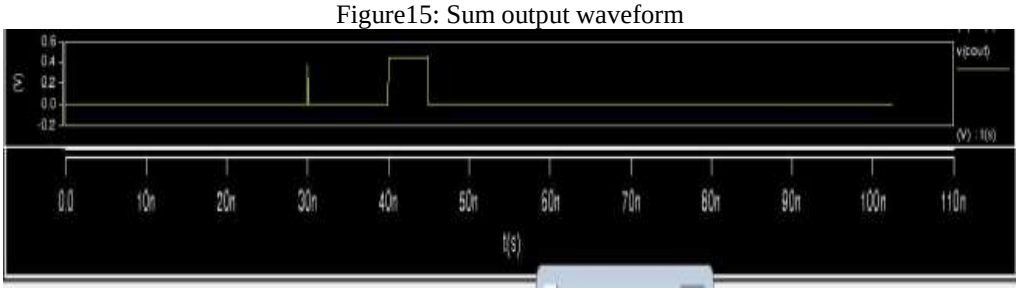


Figure16:Carry output waveformDescription:

1. If A is operated at 0v & B is operated at 0v then sum=0 and carry=0
2. If A is operated at 0.45v & B is operated at 0v then sum=0.45 and carry=0
3. If A is operated at 0.9v & B is operated at 0v then sum=0.9 and carry=0
4. If A is operated at 0v & B is operated at 0.45v then sum=0.45 and carry=0
5. If A is operated at 0.45v & B is operated at 0.45v then sum=0.9 and carry=0
6. If A is operated at 0.9v & B is operated at 0.45v then sum=0 and carry=0.45
7. If A is operated at 0v & B is operated at 0.9v then sum=0.9 and carry=0
8. If A is operated at 0.45v & B is operated at 0.9v then sum=0 and carry=0.45
9. If A is operated at 0.9v & B is operated at 0.9v then sum=0.45 and carry=0.45

5.2 SIMULATION OF TERNARY MULTIPLIER:

Below are the output waveforms of the ternary multiplier. These waveforms are obtained by using theH-spice software.

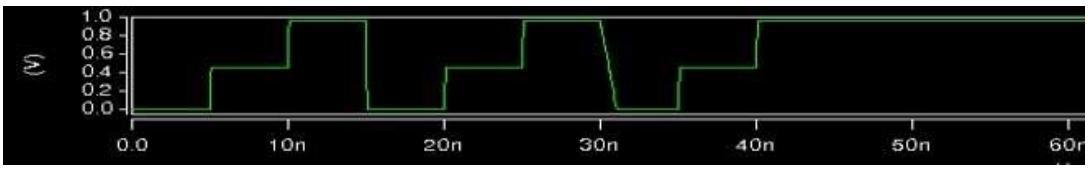


Figure17:Waveforms for the input value ‘A’ v(a)

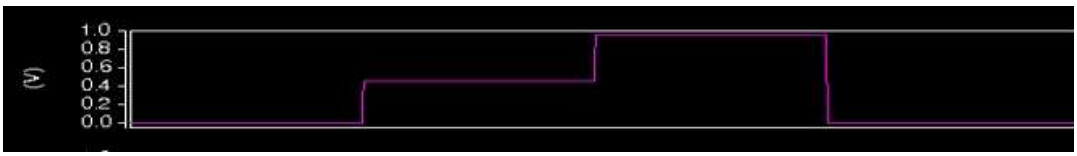


Figure 18:Waveforms for the input value ‘B’ v(b)

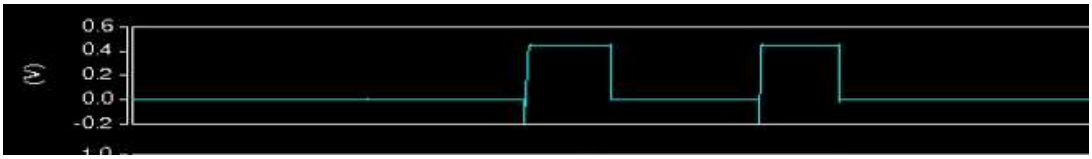


Figure 19: product output waveform

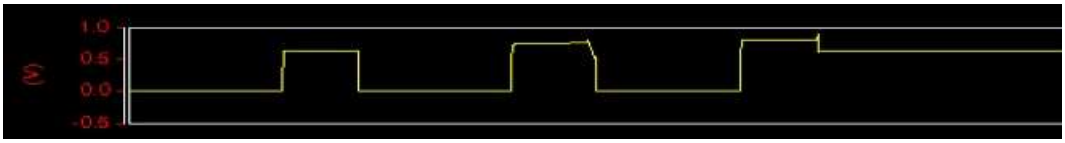


Figure 20:Carry output waveform

Description:

1 If A is operated at 0v & B is operated at 0v then product=0 and carry=0
2 If A is operated at 0.45v & B is operated at 0v then product=0 and carry=0
3 If A is operated at 0v & B is operated at 0.45v then product=0 and carry=0
4 If A is operated at 0.45v & B is operated at 0.45v then product=0.45 and carry=0
5 If A is operated at 0.45v & B is operated at 0.45v then product=0.45 and carry=0
6 If A is operated at 0.9v & B is operated at 0.45v then product=0 and carry=0.45
7 If A is operated at 0v & B is operated at 0.9v then product=0.45 and carry=0
8 If A is operated at 0.45v & B is operated at 0.9v then product=0 and carry=0.45
9 If A is operated at 0.9v & B is operated at 0.9v then product=0.45 and carry=0.45
10

VI. CONCLUSION AND FUTURE SCOPE

CONCLUSION:

This project proposes novel designs of 32 nm CNTFET-Based Ternary Half Adder and multiplier using CNTFETS. The design process utilizes different techniques in terms of transistor arrangement, two power supplies (Vdd, Vdd/2), transistor count reduction to reach the final target.

The HSPICE simulation results of the proposed circuits to existing circuits demonstrate higher performance and lower energy consumption for different simulation voltages. The results confirmed that the proposed circuits had higher robustness to process variations andhigher noise tolerance than other models. Finally, the proposed THA and ternary multipliercan be implemented in low-power nano scale embedded systems and IoT devices to save battery consumption.

FUTURE SCOPE:

The proposed ternary logic gates based THA & TMUL using CNTFET, even though its simplicity and less area make it attractive to resource-constrained IOT devices and filters but further speed we can even increase and decrease power consumption by applying Low Powertechniques to the circuits.

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