

Modeling and investigation of SET Inverter Circuit

C.Shyamala¹, V.Kalpana²

^{1,2}Department of EEE, RV College of Engineering, VTU University, Karnataka, India.

How to cite this paper: C.Shyamala¹, V.Kalpana². "Modeling and investigation of SET Inverter Circuit", IJIRE-V2I03-10-11.

Copyright © 2021 by author(s) and 5th Dimension Research Publication.
This work is licensed under the Creative Commons Attribution International License (CC BY 4.0).
<http://creativecommons.org/licenses/by/4.0/>

Abstract: This paper presents an analytical model Inverter based on the theory of single electron transistor (SET). The proposed arrangement is no doubt versatile so much that it might be used for single gate, multi-gate, symmetric, a symmetric devices and most importantly it can in like manner consider the effect of establishment charge. It can also be used for large voltage range of drain-source voltage autonomous of the tendency circumstances. The proposed design has been emulated with Flavor and the qualities produced by the proposed plan have been affirmed against Monte Carlo simulator SIMON.

Index Terms: Coulomb Blockade, Monte Carlo Simulator SIMON, Single-Electron Semiconductor

I. INTRODUCTION

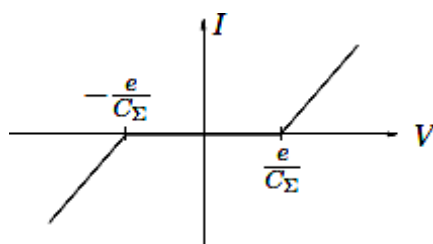
The ongoing Contraptions industry relies upon conventional MOSFET semiconductor which is a three terminal device. There are so many uses of transistors in electronics industry but the first and most important application of MOSFET transistor is a switch, which is used in essentially all electronics devices. Moore's Guideline communicates that as the years gone the no of transistors extending complex and by and by the days has come that conventional MOSFET industry is presently looking to think substitute because of the problems associated with it is increasing continuously especially leakage current which consumes the battery and nowadays all the adaptable devices are dependent on battery. To meet out these challenges Single Electron transistor comes out strongly as an alternative considering its fast working speed and low power consumption [1]. The process was started in 1968 when the process of quantization is experimented and observed in tunnel convergences. Regardless, it was in 1987 when Fulton and Dolan made the fundamental metal based SET. They made a structure by connecting two metal leads by tunnel convergences and on the top of the structure they placed an insulator and a gate electrode is placed underneath. In 1989 the first semiconductor SET was fabricated by Scott-Thomas [2]. Since then different SETs has been made with different combinations of materials. SET Inverter circuit is simulated under different biasing conditions, and for different range of temperatures. The results are differentiated and those gained by Monte Carlo simulator SIMON over a wide range of drain to source voltage.

II. I-V CHARACTERISTIC MOFSET

I-V characteristic of SET is drawn under the assumption of symmetric junction is shown in Figure 3 when capacitance And E_c is known as coulomb blockade energy. Here ΔE is the segment of the energy levels in the island. Generally the capacitance of the island is pretty much nothing and its worth ought to be $<10^{-17}$ According to condition (1) there is an extension in the EC (coulomb energy) and Increased Coulomb blockade energy is the energy of the electoral ready available in the conducting channel to another electron coming towards the channel. Thus coulomb blockade energy is responsible for $C_1=C_2$ and $R_1=R_2$. C_1 and R_1 are the source capacitance and island tunnel convergence resistance respectively. Similarly C_2 and R_2 are the channel eland resistance of drain tunnel junction respectively [6-8]. From the figure it is clearly

The Coulomb Blockade can be achieved if these criteria would meet:

1. Relationship in the bias voltage, the electronic charge and the capacitance of the channel must fulfill the following criteria:



Removed and current will flow.

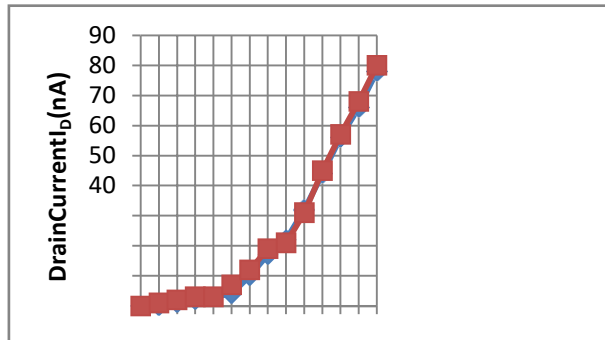
2. The Coulomb energy E_C must be greater than the thermal energy $k_B T$ i.e. $k_B T < E_C$ otherwise the electrons will pass the quantum dots simultaneously.

From, Heisenberg "uncertainty principle" i.e. $\Delta E \Delta t > \hbar/2$, the Tunneling resistance should be greater than $\hbar/2e^2$.

The flow of electrons in SET environment is basically due to the difference of the two Fermi level functions in contacts. Created by one is to keep on filling up the level(s) while made by other is to cleanse them, and as a result of this cycle there is a net movement of current from drain to source [3]. Here, all of the levels don't immediate, only some levels support the movement of electrons. The process can be seen through Fig.2.

IV. RESULTS AND DISCUSSION

Figure 6 is showing the data yield ascribes of the proposed inverter which is compared with SIMON simulator. The results of the Zing test framework are nearly same as that of the SIMON.



V. CONCLUSION

The SET Inverter arrangement has been checked against the Monte Carlo test framework SIMON. The Inverter is so arranged that it can furthermore be controlled formulate-doorway SET. It contemplates the effect of establishment charge which is the most critical wellspring of spillage current. The Inverter is implemented in the circuit test framework Flavor. Its criticism output characteristics shows an encouraging results.

References

1. Pratap Vinay, Singh Arun, Agrawal, Shyam Babu Singh, "Analytical Discussion of Single Electron Transistor", International Journal of soft computing and Engineering, Vol.-2 Issue-3 July 2012.
2. Arpan Devasi, Ritabrata Chakraborty, Arkadeep Paul, Shrabani Nayak, "Effect of equivalent circuit parameters on current-voltage characteristics in single electron transistor", International Conference on Research in Computational Intelligence and Communication Networks, ICRCICN 2016, Srivastava Anurag, Kaur Kamalpreet, Sharma Ritu, Chauhan Priyanka, Sharma U.S., Pathak Chetan, "Orientation-Dependent Performance Analysis of Benzene/Graphene-Based Single Electron Transistors", Journals of Electronic Materials, Vol. 43, No. 9, September 2014.
3. Kaur Kamalpreet, Sharma Vikash, Srivastava Anurag, "Ab-Initio Analysis of Impurity Added Benzene based multi-Island Single-Electron Transistor", Advanced Science Letter, Vol. 20, No. 7-9, July 2014.
4. Beaumont Arnaud, Dubue Christian, Beauvais Jacques, Drouin Dominique, "Room Temperature Single-Electron Transistor Featuring Gate-Enhanced ON-state Current", IEEE Electron