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Design & Power Analysis of 8T SRAM Cell

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Abstract: *This paper proposed the SRAM Architecture design using 8 Transistors to reduce the power leakages and improves the read & write delays. In the design the SRAM cell uses achargesharingtechniquebetweenthetransistorstomakeSRAMmorerigidagainstnoisesthatoccur due to low power supplies. Apart from noise reduction the read discharge power is reused. The circuit is also balanced with the same number of PMOS & NMOS, in order to achieve the maximum stability of SRAM. The comparison between standard 6T, 8T and proposed 8T with charges haring is made .Its hows that less power is consumed by 8T with charges haring than others.*

Keywords:*6TSRAM,8TSRAM,CMOS,dynamic power budge, SNM*

I. INTRODUCTION

As the device size is reducing day by day in semiconductor industry. Its impact is higher onyield, product reliability, and socost increasesdramatically. Higher performing onchipmodules and embedded microprocessors incorporate cache components or Static Random-AccessMemory(SRAM)thatplaysanimportantroleinchipsoverallreliabilityandfunctionality. The unwanted changes in SRAM circuits may lead to variations in access-time and failures in chip functionalities. From this it was very clear that the performance and costof many chips these days are highly dependent on speed and reliability of their own on-chip SRAM,scaled down feature size saffects the ON chips.

a. SRAM Memory cell operation

The SRAM cell operation is relatively straight forward.The written value is stored in flip flops which are cross coupled each other when cell was selected. Every cell was address able individually as the cells are place dinmatrix.Many SRAM memories canbe able to select entire rowatthe sametime and it also redout data present inall cells in column along with row lines.

b. SRAM Memory Applications

Inpresent days various type so fsemi conducto rmemory are available. Asperthegiven memory application choice saremade.There are mainly two type sare used those are SRAM and SRAM memory and these are useful in computer and processor sceneries. SRAM is most expensivethan DRAM.

II. LITERATURE SURVEY

a. Basic SRAM

Several SRAM cell topologies have been reportable in recent years. The resistive load four-transistor (4T) SRAM bit cell is one of the various design architectures available, which because of their symmetry in storing logic 'one' and logic 'zero,' load less 4T cells and 6 transistor(6T) SRAM cells have garnered attention in use. The leakage current of the access NMOS transistors ensures information storage within the 4T SRAM cells. As a result, they're not suitable for low-power applications. The information stability of a 6T SRAM cell, on the other hand, is free-lance of the outflow current. Furthermore, the 6T arrangement has a substantially higher noise tolerance, which is a significant benefit, particularly in scaled technologies where noise margins are shrinking. That is the primary reason why the 6T SRAM cell is preferred over the 4T variants in low-power SRAM units.

For its short time period and small size, the Six Transistor SRAM cell is the most commonly used in embedded memory. 6T cell style includes complicated choices between a variety of parameters, including abrupt area scaling, the most sensible soft error immunity ability, high cell on current, low leakage current through off transistors, and strong stability with minimal voltage and amp minimum word line voltage pulse. Figure 1 depicts the entire CMOS 6T SRAM bit cell configuration. Full CMOS SRAM configurations offer higher noise margins, lower static or leakage power dissipation, and faster change rates, making them ideal for large density SRAM arrays. Every 6T cell has the capacity to store one byte of data.
Two inverters are connected back-to-back in the 6T SRAM cell. The word line (WL) pulse controls the M5 and M6 access transistors. As long as power is available to the 6T bit cell, the cell maintains one of its two potential states, denoted by 0 and 1. In an SRAM memory cell, there are three types of operations: write, browse, and storage. The word-line is enabled to start read and write operations (WL). The value to be written is applied to the bit lines for write operations, and each BL and BLB is

recharged to VDD for browse operations. The zero storing node is upset during the browse operation, which may cause the keep data to be flipped, but the palm writes action requires that the information be flipped very quickly. Historically, device size has been chosen to balance the needs of browse and write users.

Two access transistors and two cross coupled CMOS inverters make up the 6T SRAM cell architecture. The input/output ports of the cell with high capacitive loading are known as bit lines. Only these bit lines can perform the operations READ and WRITE; we'll look at how they work. Writing style is required.

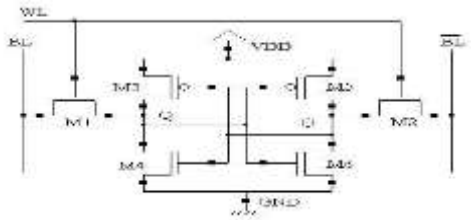


Fig1. Conventional 6T SRAM

Two cross-coupled CMOS inverters and two NMOS access transistors make up a 6T SRAM cell. The inverters' output (input) creates the internal nodes of cells A and B. Once activated, the access transistors allow the cell's internal nodes to communicate with the cell's input/output ports. Bit lines are the input/output ports of the cell unit of measurement (BL and BL.) A common data communications medium among the cells on an analogous the same column in an array of cells is measured in bit lines. As a result, they require significant physical phenomenon loading. As we come into the long run regions, the browse and write operations unit of measurement are conducted through the bit lines.

b. Read operation

A 6T SRAM cell consists of two cross-coupled CMOS inverters and 2 NMOS access transistors. The output (input) of the inverters constructs the internal nodes of the cell A and B. Once active, the access transistors facilitate the communication of the cell internal nodes with the input/output ports of the cell. The input/output ports of the cell unit of measurement called bit lines (BL and BL.) Bit lines unit of measurement a shared data communications medium among the cells on an {analogous the same} column in an array of cells. Consequently, they need high physical phenomenon loading. The browse and write operations unit of measurement conducted through the bit lines as we tend to are reaching to see inside the long run sections.

The read operation begins when the word lines (WL) are enabled, i.e. when the gate of the access transistors is turned on. Because the word lines get more intense, the power supply reaches saturation, whereas M4 runs in the thermionic vacuum tube zone. This linked with power supply has a linear relationship with the voltage of the node 'A' due to the short-channel influence. As a result, these transistors act as a resistance during this process. As a result, provide power and M4 A resistance, and raise node 'A' voltage by ΔV.

To confirm CMOS SRAM: an outline sixteen a non-destructive browsing operation ΔV is chosen in such a way that it does not trigger the M5-M3 electrical converter and node B remains at VDD throughout the cell interval. The constant resistance assumption for M4 over the interval is justified by the presence of a continuous voltage of VDD at the gate of M4.

Figure 1 illustrates the bit line discharge path's linear model. The bit line capacitance of CBL is pre-charged to VDD throughout this model. CBL discharges through power offer and M4 when power offer is activated, causing a free fall of ¢ on BL. CBL cannot discharge and remains at VDD because M1's gate supply voltage remains at zero volts (Vgs1 = 0V). To supply the regular logic levels, the respectable voltage between BL and BL, ¢, is amplified utilizing electronic equipment.

By lowering the resistance at intervals along the discharge channel, a faster bit line discharge can be accomplished. However, such improvements come at the cost of bigger cell semiconductor device sizes, which aren't always desirable for high-density SRAMs.

Traditionally, DC analysis of the cell transistors' functioning is used to verify the cell's soundness during the browsing process. Because as was previously indicated, an occasional enough ΔV ensures that the output of inverters M5-M3 at node B remains constant. The resistive magnitude relation of power supply and M4 controls the voltage level ΔV to provide a non-destructive browsing operation.

c. Write Operation

Figure 3.3 depicts the cell's behaviour during the write operation. The initial conditions of nodes A and B unit VSS and VDD are shown in this diagram. We have a propensity to focus on expanding the knowledge of the cell because re-writing recent data to the cell is trivial.

In other words, the write operation is complete when the voltage levels on nodes A and B, respectively, become VDD and VSS. If every bit line unit of measurement is precharged to VDD, the activation of the word line cannot cause a spare voltage

to grow on node A, triggering the CMOS inverter M5-M3.

As a result, the write operation is carried out by lowering the voltage on the bit line associated with node B, BL (e.g., VSS.) At the start of the process, this operation forms a possible divider consisting of M5 and power offer.
ΔV is the voltage that arrives at node B when the word lines are activated in a write operation. A sufficiently low ΔV activates the convertor M6-M4, which charges node A to VDD. Since node A is driving the M5-M3 convertor, node B is forcing all of the approach down to VSS via power offer, and M5 is turned off. As a result, the cell's logic state is altered. When the process is finished, the word line becomes inactive. A write operation is frequently bound by selecting a precise PR. At the input of convertor M6-M4, a lower PR lands up during a lower ΔV, and a lower ΔV is elaborated to higher drive.

III. 8T SRAM CELL

Circuits such as bit line pre-charge circuits and writing drivers to ensure that the bit line voltage is adjusted correctly before any operation. We tend to employ 8T SRAM cells for rapid transmission applications at low supply voltages due to the soundness constraints of 6T SRAM cells. It's similar to a 6T SRAM cell with an M5 and M6 transistor scan decoupled path.

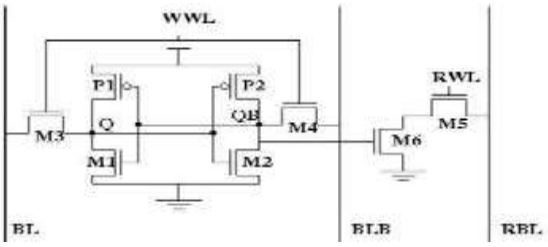


Fig3. *8T SRAM Cell*

3.1. Write Operation

The write process of an 8T SRAM cell is identical to that of a 6T SRAM cell. The following is how the write operation in 8T SRAM is carried out and discussed:

3.2. Write '0' Operation

The bit line must be given zero volts and VDD in order to write '0'. (BLbar). The write word line is asserted, causing both transistors M3 and M4 to turn on. As a result, the bit line value is saved at Q. As a result, '0' is saved at Q.

3.3. Write '1' Operation

Similarly, the letter '1' is presumably carried in the same way. The bit line must be set to VDD, and the bit line bar is set to 0 volts. Because WWL is enabled for write operations, the values in bit lines are stored at the relevant nodes, therefore at Q, the value will be logical '1' and at Qbar, it will be logical '0'. When compared to the basic SRAM process, the write operation is unchanged.

3.4. Read Operation

The read operation is started by connecting the read bit line to VDD, as in the traditional one.

3.5. Read '0' Operation

The access transistor M5 is turned on by the read word line (RWL). If the value stored at Q is '0,' transistor M6 will turn on, and RBL will be directly linked to ground via M5&M6 transistor discharges. This means that the value stored in SRAM at Q is zero.

3.6. Read '1' Operation

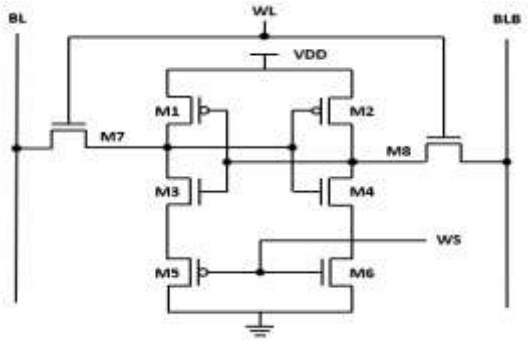
Because the M6 transistor is turned off, there is no discharge path for RBL, and the value in RBL is VDD, indicating that the value stored at Q is '1.' Figure 4 shows a circuit diagram for an 8T SRAM.
Even though the transistor count increased the power consumption, the problems of 6T SRAM are alleviated in 8T SRAM. This chapter covers the circuit diagram and operations of conventional and 8T SRAM. The next topic is the SRAM with charge sharing concept.

IV. PROPOSED DESIGN

The suggested SRAM design employs the charge sharing principle of a 10T SRAM system. The difference is that the design is done with fewer transistors than the previous 10T SRAM, which also reduces the area of the design, and we also reduced

the power consumption in the proposed design when compared to the previous design.

The proposed SRAM is made up of a single ended 7T bit cell with one bit line (BL) for write and one Read Bit cell for read operations.



During the read operation, the bit line was disconnected from the inverter pair due to WWL='0' during the read phase and RWL was enabled, resulting in M6 M5 being in the ON state. Instead of using the same BL and being pre-charged, we use a separate bit line called RBL for read operations.

Read '0'*:* When reading '0,' M4 was in the ON state, so RBL has a discharging path from M4 M5 and M6, and M6 will act like a charge sharing network, charging the bit line (BL) instead of discharging the charge to the ground, resulting in no power loss to the ground.

Read'1'*:* When reading '1', M4 was in the OFF state, so there was no discharge path for RBL to use to maintain the charge and read the '1'.

V. SIMULATIONS RESULTS

Tanner Tools 13.0 is used to design and simulate these SRAM designs using S-edit and T-Spice with TSMC018 technology. The conventional 8T SRAM and the proposed SRAM are simulated below:

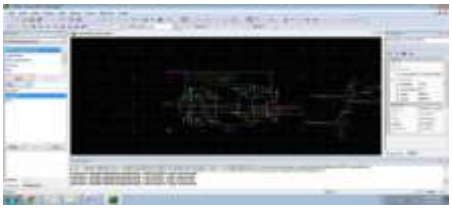


Fig5. S-edit Design of 6T SRAM Cell

Fig6. S-edit Design of 8T SRAM Cell

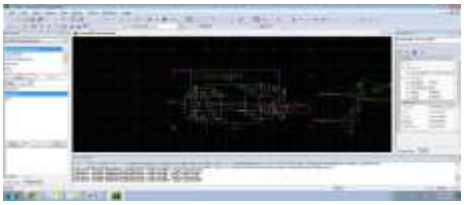


Fig7. S-edit Design of Proposed SRAM Cell

Circuit	***Power Consumption***
Conventional SRAM	5.517330e-004 watts
8T SRAM Cell	9.461892e-010 watts
Proposed 8T SRAM Cell	5.806951e-010 watts

VI. CONCLUSION

In this case, we used charge-sharing SRAM designs and analyzed them for minimum area and power consumption. The design technique will reduce power while maintaining high levels of stability.

VII. FUTURE SCOPE

We can expand this multi bit SRAM Cells in the future, and overall bit line discharge losses can be reduced by using adiabatic logics.

References

[1] *Kevin Z. Embedded Memories for Nano-Scale VLSIs. Springer Publishing Company, Incorporated. 2009; 400.*

[2] *Brown AR, Roy G, Asenov A. Poly-Si-Gate- Related Variability in Decananometer MOSFETs with Conventional Architecture. Electron Devices. IEEE Transactions in 2007; 54(11): 3056- 3063.*

[3] *Bo Z et al. A Sub-200mV 6T SRAM in 0.13um CMOS.in Solid-State Circuits Conference. ISSCC 2007. Digest of Technical Papers. IEEE International. 2007.*

[4] *Cheng B, Roy S, Roy G, Brown A, Asenov A. Impact of Random Dopant Fluctuation on Bulk CMOS 6-T SRAM Scaling. In Solid-State Device Research Conference. ESSDERC 2006.Proceeding of the 36th European. 2006.*

[5] *Singh J, Simon Hollis DKR, Mohanty SP. A single ended 6T SRAM cell design for ultra-low voltage applications. IEICE Electronics Express 2008; 5(18): 750-755*

[6] *Mizuno H, Nagano T. Driving source-line cell architecture for sub-1-V high-speed low-power applications. Solid-State Circuits. IEEE Journal of 1996; 31(4): 552-557.*

[7] *Takeda K. et al. A read-static-noise-margin-free SRAM cell for low-VDD and high-speed applications. Solid-State Circuits, IEEE Journal of 2006; 41(1): 113-121.*

[8] *Chang L. et al. An 8T-SRAM for Variability Tolerance and Low-Voltage Operation in High Performance Caches. Solid-State Circuits, IEEE Journal of 2008; 43(4): 956-963.*

[9] *Tae-Hyoung K. et al. A High-Density Subthreshold SRAM with Data-Independent Bit line Leakage and Virtual Ground Replica Scheme. In Solid-State Circuits Conference. ISSCC 2007. Digest of Technical Papers. IEEE International. 2007.*

[10] *Wang X, Roy S, Asenov A. Impact of Strain on the Performance of high k/metal replacement gate MOSFETs. Proc. 10th Ultimate Integration on Silicon (ULIS 2009), 2009.*