International Journal of Innovative Research in Engineering
Volume 4, Issue 2 (March-April 2023), PP: 500-513.
www.theijire.com ***ISSN No: 2582-8746***

A Pencil-Shaped 9- Level Multilevel Inverter

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How to cite this paper:
ROJA R[1], Dr Sivaprakash JS[2]
, "A Pencil-Shaped 9- Level Multilevel Inverter", IJIRE-V4I02-500-513.

https://www.doi.org/10.59256/ijire.2023040220

Abstract: *It is suggested to build a 9-level pencil-shaped (PS) inverter with a minimum of two DC supplies. Low component multilevel inverters (MLIs) employ extra conducting switches in addition to the DC supply.*

- *This suggested MLI is more effective since it uses fewer power electronic switches. The architecture enables a higher voltage level inverter with a modular design that uses fewer DC supplies and does it appropriately without the need for an additional H-bridge circuit. Additionally, a control plan is suggested for distributing loads equally in a nine-level architecture.*
- *The potential for equitable load distribution in higher-level designs and fundamental frequency switching of switches carrying larger voltage strains are also being looked into. Through simulations and experimental experiments, several notions are validated. The simplified formulae for the suggested inverter parameters are built to determine their optimal capabilities.*
- *Additionally, an optimal PSMLI design is created using the expanded model of the suggested architecture to reduce the inverter's total standing voltage (TSV). Comparison studies are provided to support the proposed inverter and show its benefits over recent MLIs of comparable sorts.*
- *Through accurate simulation and lab tests, the MLI was able to achieve a greater efficiency of 95.54%. The improved 17-level version of PSMLI, on the other hand, achieved IEEE 519 standard performance with total harmonic distortions (THD) of just 5.15%.*

Key Word: *Multi-level inverter, power electronics, switched capacitor, voltage boost, nearest level control.*

I.INTRODUCTION

- Multilevel inverters have a reliable and efficient output voltage. MLIs with a variety of forms is a favourite among researchers in the field of power electronics. Regarding MLIs having a unique form.
- In recent years, power systems have evolved into a wide variety of designs with diverse applications. In this study, a tiny pencil-shaped (PS) 9-level inverter that used just two DC inputs is analysed.
- A lot of the low-component multilevel inverters (MLIs) that have been proposed make use of extra conducting switches and improperly managed DC sources.
- The literature that is currently accessible contains generalizations of topologies with symmetrical sources, but no study has been done on equal load distribution and asymmetrical configuration.
- MLIs can be classified as asymmetrical, symmetrical, or hybrid depending on the layout and dimensions of the DC supply.
- Due to the utilization of four DC sources, galvanic isolation will need to be provided by four transformers, which might greatly raise the system's overall cost.
- As a result, employing asymmetric DC sources necessitates exact voltage balancing to maintain the DC sources' voltage ratio, which might add to complexity management.
- The suggested MLI required just 10 switches and two symmetric DC sources in comparison to providing a 9-level voltage. With the use of two switching capacitors, two DC supplies, and nine output levels, this module can provide sinusoidal voltage. A new generation of switched capacitor MLIs operates without the use of DC sources.
- MLI (SCMLI) has been utilized to decrease the number of components. However, this also reduces switching stress. This specific MLI group has evolved by utilizing a mix of capacitors and DC power sources.
- The proposed module is capable of producing a negative output level without the use of a separate circuit. The TSV of the MLI can be decreased as a result.

1.2 What is a Multilevel inverter?

- Currently, the power sector is very interested in multi-level inverters. A sinusoidal voltage is often created by combining several levels of regions that are derived from a capacitor voltage source. In addition to having high power ratings, these

inverters make it possible to employ renewable energy sources including solar, wind, and fuel cells.

- With regard to high-power operations, the multilevel inverter has drawn greater attention. Recently, it has been able to transition between high switching frequencies and lower-order harmonic components. The waveform becomes increasingly sinusoidal and has less harmonic distortion as the number of levels rises. Voltage levels rise as the number of layers rises.

1.3 Features of Multilevel inverter:

- Very little distortion and a low rate of voltage change have been produced.
- The huge voltage transients are automatically rectified by it.
- They can function at extremely low switching frequencies and produce very little distorted input current

1.4 Types of Multilevel Inverters:

1. Diode clamp multi-level inverter
2. Flying capacitor multi-level inverter
3. Cascaded multi-level inverter

1.4.1 Diode clamp multi-level inverter:

- A diode lamp multi-level inverter generates m levels of phase voltage and is made up of m-1 capacitors on the DC bus. With the use of clamping diodes, the switch's maximum preventing voltage will be constrained to one capacitor voltage level. Different switches have varied switching times depending on the duty cycle and time on the duty cycle and time, different switches have varied switching times.

1.4.2 Flying capacitor multi-level inverter:

- It is the same as a multi-level diode clamp inverter. An m level has m-1 capacitors with voltage level steps of 2m-1 for the phase voltage. Real power transfer may employ consist of switch configurations. The main issue with switch-modified selection and frequency operation is that it is greater than the fundamental frequency. Harmonic content decreases as the number of voltage levels rises. To create the zero voltage level, the load cannot be directly coupled to the converter's ground.

1.4.3 Cascaded multi-level inverter:

- Three voltages are linked in a star or delta for a three-phase cascaded. It is made up of a unique DC source that can be adjusted for different renewable energy sources like solar, fuels, biofuel, etc. To order to prevent large resistor-capacitor pairings, easy switching may be an option.
- Multi-level inverters are the basis of an increasing number of commercial products today, and perhaps more instrument measures are being done on them.

1.5 Key Reasons behind the ability of MLIs:

- MLIs have a modular design.
- Due to flexibility, high current and voltage capabilities are possible.
- Due to the separation of voltage stress among switches at various levels, semiconductor switches' voltage derivatives have been reduced.
- By adopting the proper switching techniques, common mode voltages in electric drives and solar PV applications may be reduced or eliminated.
- Due to the output waveform's various levels, it performs competently in terms of power quality (low THD output).
- Ability to operate without a transformer.
- Higher efficiency levels result from switching at the fundamental frequency, which lowers switching and conduction losses.
- The fault-tolerant operations employ appropriate control strategies and make use of many redundant switching states.

II.REVIEW OF LECTURE:

- A thorough analysis of some of the more modern multilevel inverter topologies with the aforementioned goals is provided. This article presents the results of a thorough examination of the overall number of semiconductor switches, the number of DC sources, the demand for passive components, the greatest switch voltage rating, the total standing voltage, etc.
- Based on the characteristics provided, many new suggested MLI topologies with a lower device count are examined and debated. All architectures are demonstrated using their suggested module structures and building methods, assuming four DC input sources.
- Comparing the proposed PSMLI module to existing MLIs found in recent research, less powerful electronic components are used.

Objectives of the research:

- Without any extra power sources, it can naturally create negative voltage using its sophisticated switching structure and current channels. As a result, the TSV of the PSMLI has drastically dropped.
- The suggested MLI uses a clever mix of switches, V_c, and DC-links to provide multilayer voltage with fewer switching transitions.
- The capacitor voltages can be balanced by the proposed MLI without the use of any extra power components. As a result, the structure has been further improved and made simpler, making it more efficient.

Problem Statement:

- Take the example of a two-level inverter first. A two-level inverter produces two separate voltages for the load; for example, if we supply Vdc as an input, it will produce + Vdc/2 and - Vdc/2 on the output.
- These two freshly created voltages are often swapped in order to create an AC voltage. The most common switching method is PWM.
- Although this technique of producing AC is efficient, it has certain downsides, including a higher DV/DT than a multilayer inverter and harmonic distortions in the output voltage.
- Although this approach typically works, there are a few instances where it doesn't, especially where minimal output voltage fluctuation is desired.

Research methodology:

- The proposed PSMLI module uses fewer power electronic components. It can naturally generate a negative voltage without additional power components because of the need for extra power components because of its clever switching arrangement and current paths.
- The TSV of the PSMLI has dramatically lowered in response. The suggested MLI generates multilayer voltage with fewer switching transitions by cleverly combining switches, switched capacitors, and DC connections.
- The capacitor voltages do not need to be matched by any extra power components in the proposed MLI.
- The entire manuscript's structure is arranged by segments. This covers qualities like modularity, TSV, efficiency, and power. The work's whole framework has been set up. We discuss the TSV, PSMLI's modularity, its capabilities, efficiency, and power losses.

Research Analysis:

- In this part, a thorough comparison of PSMLI with conventional and other newly suggested MLIs is offered in order to demonstrate PSMLI's superiority in terms of the utilization of less powerful electronic components.
- For each MLI, the symmetrical variant is chosen for comparison. Since configuration-2 of PSMLI is more optimised than configuration-1, it is chosen for this investigation.
- The following variables were selected to compare: the total number of DC sources (NDC), the total number of power switches (NP), the total number of voltage levels (NV), the maximum voltage (NVmax), the total switching volume (TSV), the boosting factor, and the necessity of an H-bridge circuit.
- The suggested MLI uses less power switches than the traditional MLIs, as can be seen from the comparison. Compared to PSMLI, the traditional NPC inverters require less DC sources.
- However, a significant number of switches are needed. generating higher voltage levels by clamping diodes and capacitors.
- As a result, it has significant voltage imbalance concerns that need to be fixed using sophisticated modulation techniques.
- Although FC MLIs need only a few DC sources, they have the drawback of utilizing a lot of capacitors and power switches, which can significantly reduce the MLI's efficiency by causing capacitance losses in the system.

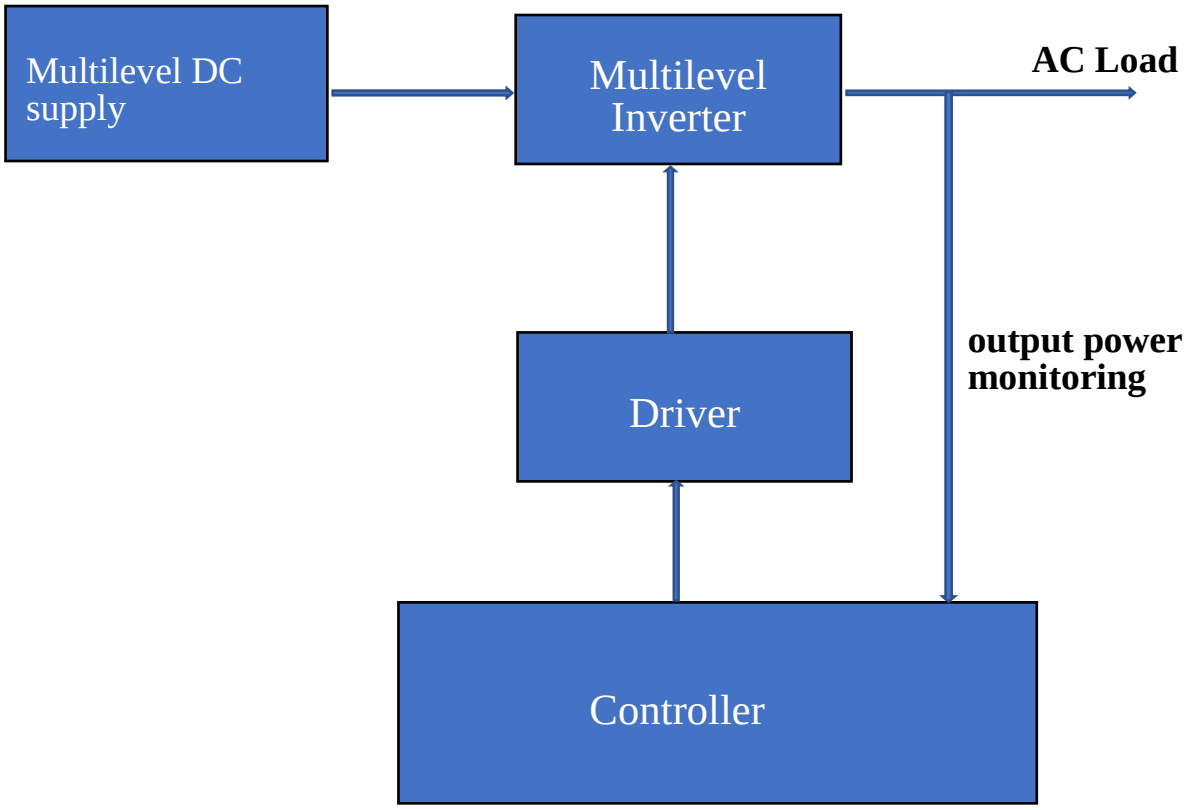
- Additionally, compared to PSMLI, the TSV of the CCMLI is 42VDC, a significant increase.
- The MLIs that have been suggested share a similar characteristic. when more switches and DC sources are needed than in the case of PSMLI.
- For the default setup, the proposed MLI needs one switch, the same number as the PSMLI.
- However, when the voltage level rises, they need more DC sources and switches, which is visible. They do, however, need a lot of power switches.
- Additionally, it is clear that the boosting factor only applies to MLIs made up of switched capacitor units.
- This gives these MLIs an extra benefit because they don't need a lot of converters and segregated DC sources. It offers the biggest boosting factor.
- To generate a 9-level output at n = 1, both of these modules required a single DC source.
- The SCMLIs that have been proposed, however, have the capacity to quadruple boost.
- Although these MLIs have a larger boosting capacity than the proposed MLI, it is clear that they have also generated a high TSV and used a large number of power switches.

- Thus, it is possible to claim that the suggested PSMLI has achieved a balance between the use of power electronic components such as switches and boosting ability, and TSV.
- Evaluating PSMLI to other MLIs in terms of power losses and efficiency serves to further demonstrate its superiority. The PLECS software is used to calculate power losses and efficiency.
- To support the comparison, identical models of power electronic switches, DC sources, diodes, and capacitors were used in the construction of the MLIs.

- Additionally, for the MLIs with an operational power of 900 W, a maximum DC-link voltage of 200 V is taken into account.
- Three types of losses—conduction losses (Pcon), switching losses (Psw), and capacitor losses—are taken into account when calculating the efficiency () of each MLI (Pcap).
- The total power losses (Ptotal) of each MLI are then calculated using the data on power loss acquired from PLECS software, which shows that PSMLI has a lower efficiency.
- This is because there is no capacitor loss because there are no capacitors built into these MLIs. However, each of these MLIs uses a number of DC sources, which significantly raises the cost of construction.
- It should be mentioned that the efficiency of the SCMLIs is determined for producing 7-level voltage. However, the suggested MLI is more effective than any SCMLI.

Findings:

III.BLOCK DIAGRAM



2.1 Block diagram of MLI

3.1 Block Diagram Description:

- The proposed MLI receives several dc inputs.
- MLI was altered to provide an output of nine levels.
- There is less harmonic content as a result.

3.2 PSMLI and its configurations:

- The suggested module uses switched capacitors and a carefully chosen arrangement of DC sources to the output voltage with greater possibilities to obtain.
- This architecture leverages switched capacitors' fundamental mode of operation to boost and further raise the voltage levels.
- Maintaining the capacitors' voltage without needing an extra circuit would be difficulties needed for an extra circuit would be difficult for this form of MLI.

3.3 Applications of MLIS:

- The use of multi-level inverters for lower voltage, high power purposes has evolved from technological innovations to a proven, appealing option.
- Multi-level inverter advancements may be further motivated by the ongoing advancement of technology and the evolution of industrial applications, which will present new problems and possibilities.

IV.SCHEMATIC DIAGRAM OF MLI

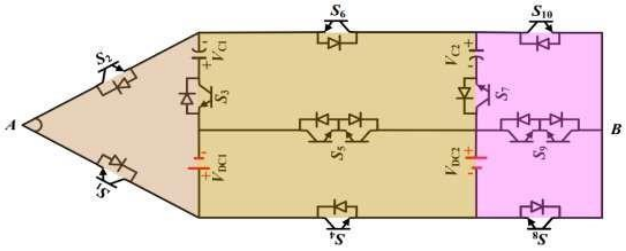


Fig 4.1

- It has 3 principal segments which are represented using 3 color schemes.
- The first part is called the head (brown color)
- The 2nd segment is referred to as the body(yellow color) and
- The eraser is the final part (pink color).
- They are ten switches are used. In that,
  1. Unidirectional switches - S3,S4,S5,S6,S7,S8,S9,S10
  2. Bidirectional switches - S1, S2.
- DC source – V_{DC1},V_{D2}.

- Switched capacitor- V_{C1}, V_{C2}.
- Mosfet as a switch is used here.
- They are ten types of flow to get the output voltage.
- Based on the switching pattern it will operate.
- The operation slowly increases the level of voltage.

4.1 Mosfet:

- In a field-effect transistor (FET with an insulated gate), known as a metal-oxide-semiconductor field-effect transistor (MOSFET, MOS-FET, or MOS FET), the voltage controls the device's conductivity.
- Signals can be switched or amplified using it. The ability of materials to change their conductivity in response to the amount of applied voltage allows for the amplification or switching of electronic signals.

4.2 DC Source:

- DC enables a gadget to receive a steady stream of current. Power must be transformed from AC to DC because it is first given as AC.
- To work with an AC-to-DC converter from wall power, the majority of smaller electronic equipment (such as PCs) needs direct current.

4.3 Switched Capacitor:

- A switched capacitor (SC) is an electrical circuit that carries charges into and out of capacitors in response to the opening and closing of electronic switches.
- The switches are often controlled by non-overlapping clock pulses to ensure that not all switches close at once.
- Switched-capacitor filters are those that use these components as opposed to exact resistors and depend exclusively on the ratios between capacitances and the switching frequency.
- Because they can be constructed more affordably, they are significantly more appropriate for use in integrated circuits than precisely defined resistors and capacitors.

4.4 Working Principle of PSMLI

- Two unidirectional switches are included in the first part (S1, S2,). These act as directional switches, determining the module's current course.
- For instance, PSMLI only generates positive voltage levels when S1 is turned on. S2 can, though, often produce negative voltage levels when it is powered on.
- The body section is made up of 2 DC sources (V_{DC1}, V_{DC2}), 4 unidirectional switches (S3, S4, S6, S7), 1 bidirectional switch (S5), and 2 switched capacitors (V_{C1}, V_{C2}).
- A bidirectional power switch (BPS) is an active switch that, when turned ON, may permit bidirectional current flow and, when turned OFF, can prohibit bidirectional voltage flow.
- To prevent the capacitors V_{C1} and V_{C2} from short-circuiting switches S3 and S7 are used.
- Filters that rely only on the relationship between capacitances and the switching frequency are known as switched-capacitor filters since they employ these parts rather than precise resistors.
- Between the head and the eraser, the body section serves as a conduit. The bidirectional switch S5 prevents the reverse current from flowing.
- PSMLI has an eraser-shaped bottom. It has a T-type inverter-like structural design and creates negative levels without the use of an extra H-bridge unit.
- Using the DC connections, the MLI can generate a 9-level voltage (4 level and 0 level).
- The power switches used by PSMLI are carefully designed such that the capacitors and DC supply are connected through several current channels, eliminating the need for an extra circuit to balance the capacitors' voltage.

4.5 Psmli's Switching Pattern:

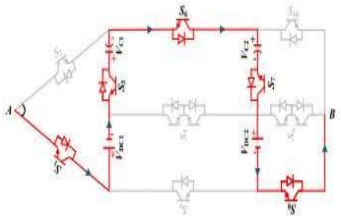
Output		Pattern of switching									
	V_{AB}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}
+Levels	$4E$	1	0	1	0	0	1	1	1	0	0
	$3E$	1	0	1	0	0	1	1	0	1	0
	$2E$	1	0	0	0	1	0	0	1	0	0
	E	1	0	0	0	1	0	0	0	1	0
$+V_{C2}$	0(i)	1	1	0	0	1	1	1	0	0	0
$+V_{C1}$	0(ii)	0	0	1	0	1	1	0	1	0	1
	$-E$	0	1	1	0	1	0	0	0	1	0
-Levels	$-2E$	0	1	1	1	0	0	0	1	0	0
	$-3E$	0	1	1	1	0	0	0	0	1	0
	$-4E$	0	1	1	1	0	0	1	0	0	1
Number of turn on in each cycle		1	3	2	1	2	3	4	7	8	3

Table 1

- This switching pattern has 4 positive levels and 4 negative levels.
- According to this pattern, only the PSMLI's current path produces the 9-level voltage.
- The power switching component of this PSMLI uses the nearest level control(NLC) technique.

- The NLC technique is the identification of the submodules that may be done at various stages of the execution of this approach after the submodules are sorted according to the number of submodules that will be turned on.
- Additionally, the individual submodule status in the gate pulse generating step is not necessary with the suggested solution.
- The switching states of the voltage levels may be used to build the gate logic in the proposed manner.
- The suggested balancing method's simplifications and removal of several phases may make things easier and need less processing time during implementation.
- Table 1 also shows the number of cycles that is the number of times each switch turns on during the operation of one complete cycle.

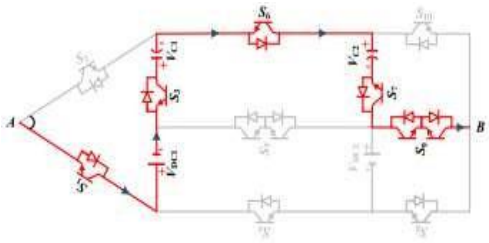
Level 0:



- The highlighted red color shows the current flowing path.

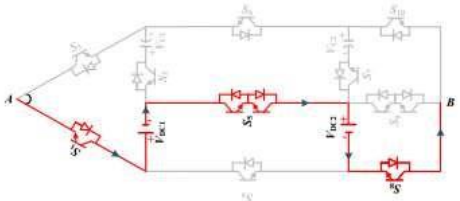
- From the A the current passes to S1 unidirectional switch then it enter into VDC1.
- Further the current flows to S3, VC1, S6, VC2, S7, VDC2, S8, and finally to B.
- The flows are happens according the PSMLI Switching pattern of Table 1.
- For 1st level V_{AB} =4E.
- Likewise for all other 9 levels current flow will happen.

Level 1:

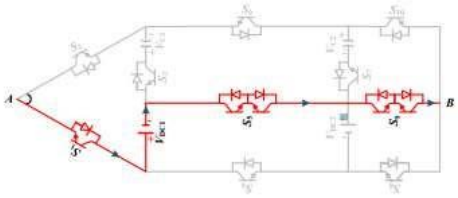


- According to the PSMLI Switching pattern current path is produced.
- In this S9 bidirectional switch takes place. An active switch with the capacity to block current in both directions is referred to as a bidirectional switch.
- V_{AB}=3E

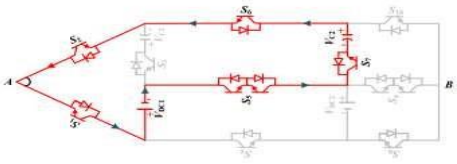
Level 2: V_{ab}=2e



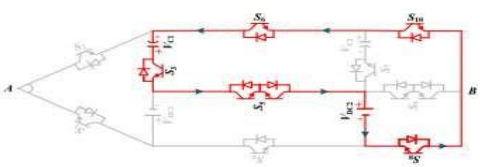
Level 3: V_{ab} =E



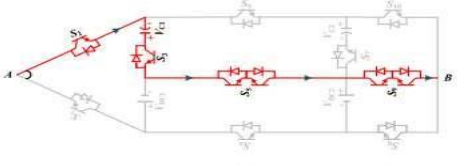
Level 4: V_{ab} =0(+Vc2)



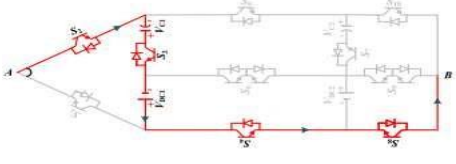
Level 5: V_{ab} =0(+Vc1)



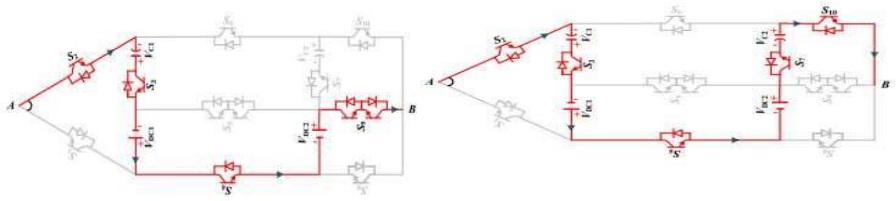
Level 6: V_{ab} =-E



Level 7: V_{ab} =-2e



LEVEL 8: V_{AB} =-3E LEVEL 9: V_{AB} =-4E



- These are the current path to produce 9-level voltage.
- Based on Table 1 the current passes through the circuit.
- According to Table I's switching sequences, switches S1, S2, S3, S4, S5, S6, and S10 are spinning with a low frequency, which has greatly lowered the TSV of the PSMLI.
- A graphical representation of the TSV of each switch for each voltage level of PSMLI is provided. The TSV of the PSMLI is therefore determined to be 16 VDC.

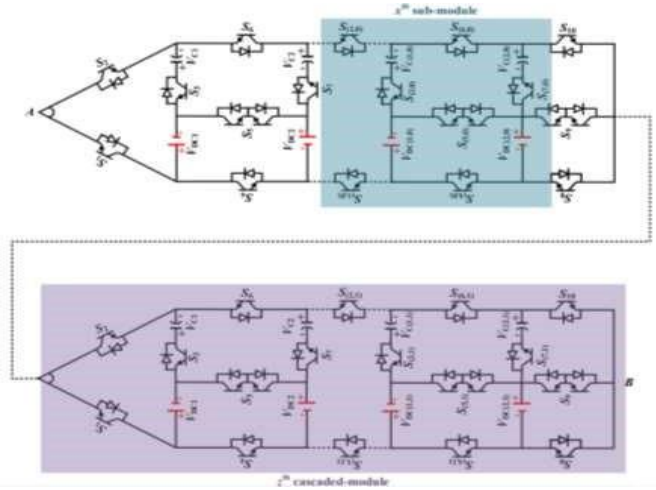


Fig 4.2

- To increase module's ability to produce electricity, a cascaded connection is formed. Six unidirectional switches, one bidirectional switch, two switched capacitors, and two DC sources are all included in the xth submodule.

- Despite the fact that asymmetrical MLI structures introduce unnecessary voltage stress and imbalance into the system, they are one of the most straightforward ways to raise voltage levels without adding any structural complexity or using more powerful electric components.

- Asymmetrical modules can be used to extend the proposed PSMLI as well. The second submodule of the PSMLI is built with voltage sources capable of tertiary voltage (VDC(1,0) = VDC(2,0) = 3E), or, in other words, a voltage ratio of 1:3 is maintained between the original module and the expanded module, in order to maximize the voltage level.

- Thus, the enlarged PSMLI would be able to provide 33 voltage levels with the addition of just 8 switches.

- The PLECS programme is used to evaluate the efficiency and power loss of the proposed MLI setup. All heat sinks are evaluated for the power loss in steady-state conditions with an ambient temperature of 25°C.

- The heat sinks receive heat equally from all directions. The thermal profiles of diodes and IGBTs are automatically calculated by PLECS software utilising the data sheets.

- The heat sinks receive heat equally from all directions. The thermal profiles of diodes and IGBTs are automatically calculated by PLECS software utilising the data sheets.

- Under typical working conditions, the PSMLI is expected to lose 900W of power.

- The efficiency is estimated by accounting for the power losses of switched capacitors as well as the conduction and switching losses of switching devices.

- The dissipating factor is represented by tan 0, which is 0.15, and C, which stands for the capacitance, represents the fundamental frequency, which is 50 Hz. The capacitor losses are 11.8 W using (18) - (20).

- In comparison to the overall switching and conduction losses of the IGBTs, the switching and conduction losses of the diodes are 0.012 W and 0.871 W in steady state, respectively. 94.5% overall efficiency and a 22.063 W overall power loss are the results.

- A steady total DC-link voltage is required for an excellent AC output. A switchable capacitor must have a voltage ripple of no more than 5% in order to prevent a substantial quantity.

- This establishes that the capacitor voltage has minimal ripples, and the suggested MLI can be applied successfully.

4.6 Optimized PSMLI Topology:

- The TSV of the extended symmetrical PSMLI can be decreased by selecting the best structure for each module.
- The asymmetric PSMLI is not taken into account in this case due to the disadvantages of such modules, such as their high TSV and voltage imbalance, which may be quite problematic, particularly in applications involving renewable energy.
- To create the suggested PSMLI's expanded structure with the least amount of voltage stress, a certain arrangement of x (submodules) and z (cascaded modules) must be adopted.
- Additionally, this ideal arrangement makes sure that less power electric components are completely employed.
- In order to determine the best configuration, the voltage levels (NV) and accompanying TSV for two distinct PSMLI topologies can be shown.

4.7 CONFIGURATION 1:

- Any number of cascaded or zth modules with one cross-connected submodule in each can be used to create a PSMLI (x = 1).
- The number of voltage levels that the proposed inverter can generated, which is 8z + 17. On the other hand, by using, it is possible to determine the TSV of the entire inverter.

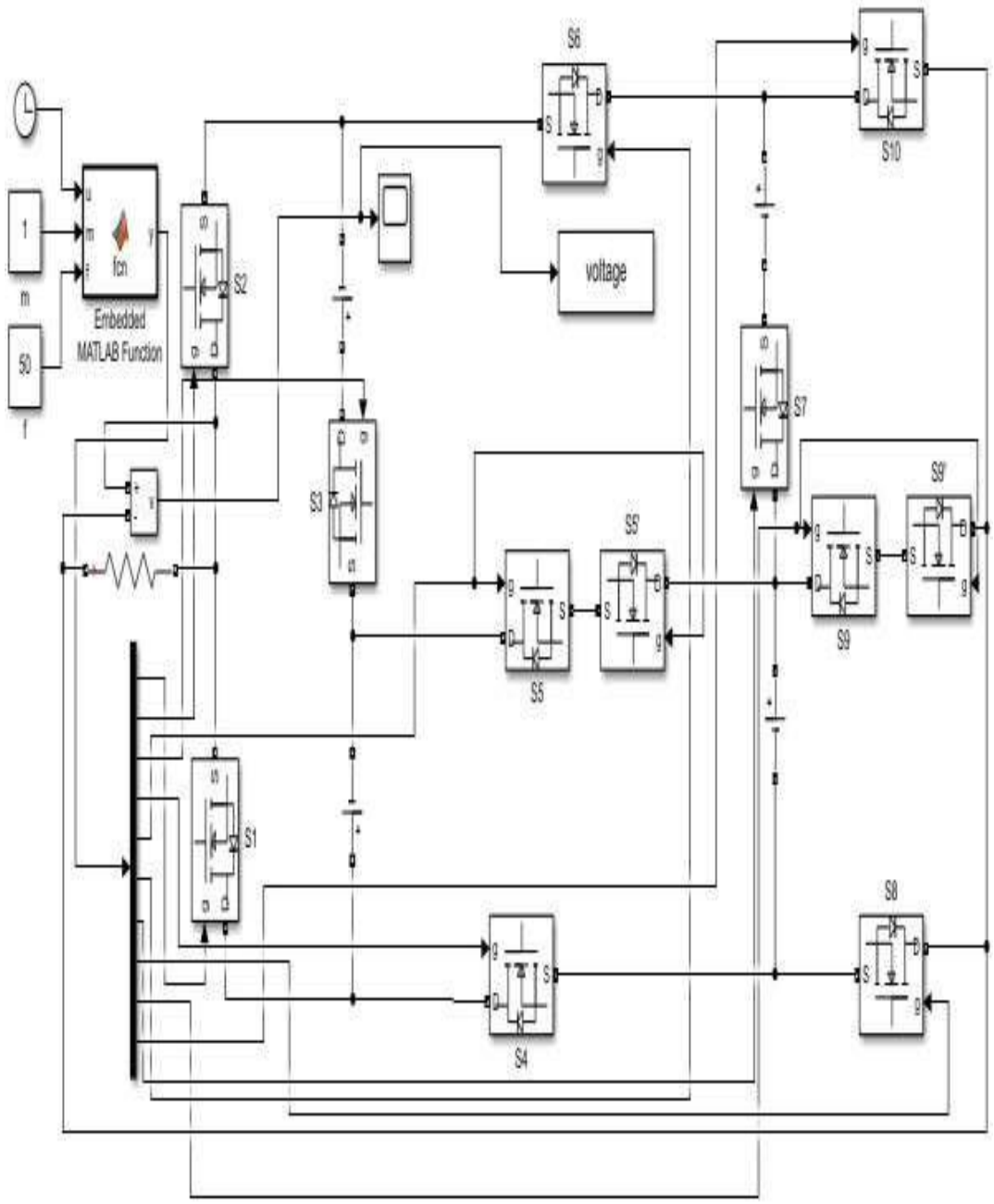
4.8 CONFIGURATION 2:

- In this arrangement, the PSMLI can be created with a single cascaded module (z) and a number of submodules (x > 1).
- Under these conditions (configurations 1 and 2), (3) and (4), respectively, may be used to calculate the quantity of voltage levels (NV) and TSV of the unique MLI. The visual comparison between NV and TSV.
- It is clear that configuration 2 is more practical than configuration 1 in terms of TSV. The use of 4 more switches together with the addition of several cascaded modules is the cause of configuration 1's increased THD.
- Since switches with high voltage ratings are quite costly, configuration-1 will have a substantially greater total cost than configuration-2. However, configuration-1 is preferred in terms of simplicity and switching control.

- Because it may be constructed using the same switching patterns and comparable cascaded components.
- Configuration 2 is more economical in terms of power switches since it has Higher voltage levels that can be generated with fewer power switches.
- While configuration-1 needs 112 power switches to create the same voltage level, configuration-2 can do it with just 84 power switches.
- Taking into account all of these positive characteristics, this text places greater attention on configuration 2.

V.SIMULATION RESULT

- The Simulation of the Multilevel inverter was carried out using MATLAB Simulink. The was designed using the basicelectrical toolbox components.
- The simulation was executed and the performance of the inverter was analysed and the results were tabulated and waveforms were noted.
- The parameters which were studied are input current, input voltage, output current, output voltage, AC side power factor and Total Harmonic Distortion. To observe the THD, the FFT analyser tool was used to monitor the magnitude of each Harmonic component.



- This part demonstrates the versatility of the planned PSMLI by generating a greater variety of voltage levels.

- This is accomplished by expanding the 9-level PSMLI inverter's structure, which is shown. In this case, there is a 1:1 ratio between the DC sources and the capacitors.
- The body component of PSMLI is expanded to create the extended structure, which is then joined to some other structure similar via cascaded connections.
- Two conduit switches that are positioned between the PSMLI's main body and stretched body convert the polarity.
- Identical to the directional switches utilized in the head part of the PSMLI, these two switches will also serve as polarity converters.
- Input voltage- 270V
- Resistor- 10 Ohms
- Frequency- 50Hz
- From the input Voltage and resistor we can calculate the current and power of the MLI.
- The Functions of the components we used in the Matlab are
- The mosfet acts as a switch to control the conductivity or how many electricity can flow.
- Embedded MATLAB function used to convert the wriiten m-code to the S-function.
- Constant use to initialize the specific vales of the block which cannot change.
- Therefore, the output voltages are and other important details are measured on their specific components.

5.3 Simulation output:

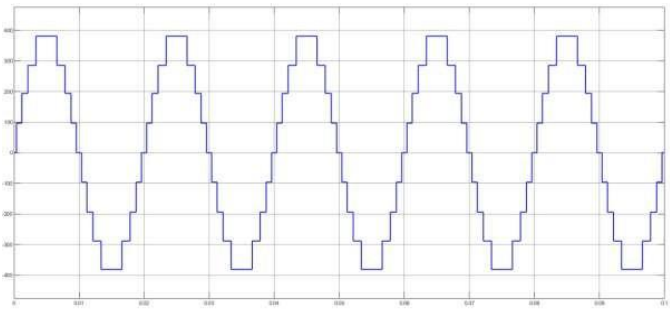


Fig 5.1

- MATLAB The planned PSMLI is simulated using Simulink.
- This is the graph between time and voltage.
- In according, the PSMLI table configuration level by level voltage is increased.
- For nine level furtherly, voltage is increased.
- The operation of the proposed PSMLI is validated.

5.4 Harmonic Order

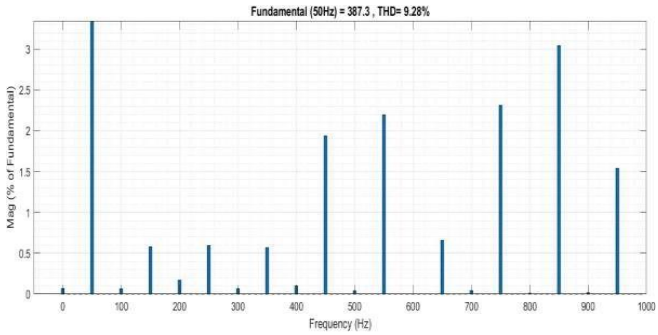


Fig 5.2

- The NLC modulation approach is used the PSMLI's 9-levels (n = 1) output voltage.
- Here, each voltage level is 100 V, resulting in an output voltage of 400 V from a multilevel staircase running at 50 Hz.
- The nine-level output voltage's harmonic spectrum is shown. Furthermore, the cascaded PSMLI's harmonic spectra and output voltage at 17 levels (n = 2).
- This cascaded module can provide an output voltage of 80 V while maintaining the same individual voltage level of 100 V.

17-Level MLI:

By raising the inverter's level, the overall harmonic distortion may be reduced, allowing us to use more levels to achieve the optimum output with the least amount of distortion possible.

Output Waveform:

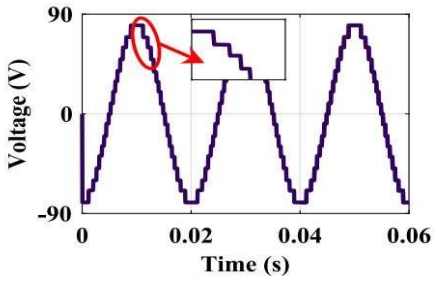


Fig 5.3

Harmonics Order 2:

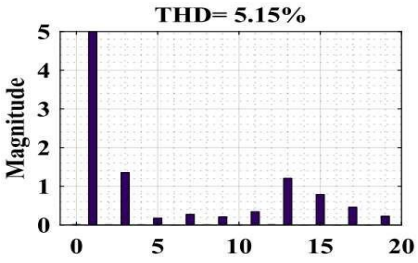


Fig 5.4

- This Harmonics order of 17 level inverter THD is 5.15%.
- The overall distortion is reduced by increasing the level.
- In the 9 level multilevel inverter the THD value is greater than the 17 level inverter.
- Therefore, this shows that by increasing the level the distortion will reduce.

VI.RESULT

- Therefore, for the by using the Matlab Simulink the proposed PSMLI is used.
- For 9-levels the illustration of fig 5.1 using NLC modulation technique is obtained.
- Here, the output voltage of the multilayer staircase is 400 V, with each voltage level being 100 V.
- The output voltage's harmonic spectrum for the nine levels is shown.
- Additionally, the harmonic spectra and output voltage of the cascaded PSMLI, which has 17 levels (n = 2).
- This cascaded module, which has separate voltage levels of 10 V, can provide an output voltage of 80 V.
- By assuming the same limitations in both models, the simulation revealed that the total harmonic distortion of a nine-level inverter was approximately 9.28% and that of a 17-level inverter is 5.25%.
- For low power ratings, nine level inverters are utilised, whereas 17 level inverters are used for large power levels. By raising the inverter's level count, the number of switches needed will rise; for example, a 9-level inverter has fewer switches than a 17-level inverter.

Limitations of Research:

- Additional component count
- For some setups, more than one isolated DC supply is required.

VII.CONCLUSION

We may infer from the entire discussion above that a multilayer inverter architecture with an appropriate switching angle and calculated conduction duration is necessary.

By adding a harmonic filter with the appropriate frequency, we can remove a significant number of harmonics and lower THD, at least in software-based simulations.

Therefore, we have finally achieved the THD level of 9.28% by utilising suitable switching angles and by using a filter, which shows that the waveforms are closer to the basic sinusoidal waveforms.

Power rating can be raised by expanding the inverter's range of voltage levels without raising the requirements for specific devices.

Multilevel voltage source inverters' distinctive design enables them to achieve high voltages with minimal harmonics without the use of transformers or devices connected in series for synchronised switching. The output voltage's harmonic content is greatly reduced.

With the help of MATLAB/Simulink, the Sinusoidal Pulse Width Modulation Technique is used in this project's simulation of a nine-level inverter. A nine-level inverter is used in this project to create seventeen of the AC output voltage. This experiment examined the efficiency and losses of a seventeen-level inverter. When the findings of a previous simulation of a nine-phase, three-level inverter were compared to those of a seventeen-level inverter, it was discovered that the overall harmonic distortion had decreased by 4.21% and the efficiency had risen by 2.44%. THD lowers and active power increases as the number of levels rises.

Both the voltage and load current output waveforms resemble sine waves.

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